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Military EMBEDDED SYSTEMS

VOLUME 7 NUMBER 4
JUNE | 2011

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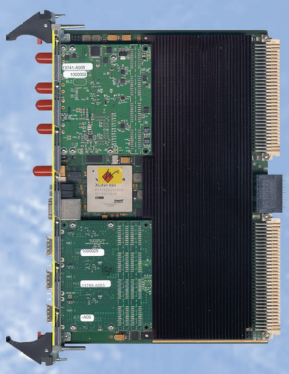

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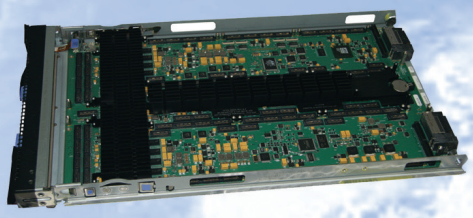

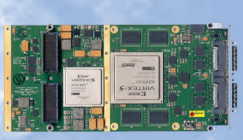

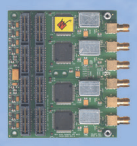

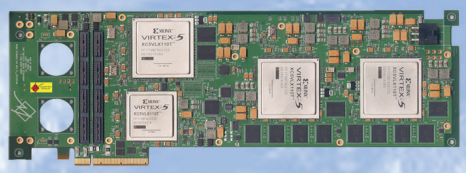

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Military EMBEDDED SYSTEMS

June 2011 Volume 7 Number 4

COLUMNS

DEPARTMENTS

ON THE COVER:
On the cover: Talk about legacy platforms! The U-2 Dragon Lady spy plane first flew over the USSR in 1956, practically the only sensor platform the U.S. had for ISR at that time. The B camera (inset) offered 7 pivot positions and wound thousands of feet of high-speed film. Today, UAS drones, DSP-enabled sensor fusion, and COTS "desktop" CPUs make the U-2 look like a relic. Yet it still flies today with upgraded sensors and allegedly participated in operations over Libya. But legacy challenges still hamper the military. In this special issue, we look at UAS platforms, the changing face of ISR, and how to counteract the threat of counterfeit legacy components. (Images courtesy of the U.S. Air Force, as posted on Wikipedia Commons.)

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CORRECTION: In our MES May edition's Editor's Choice award to RTI for its DDS Technology Network, we said, "According to RTI, more than 200 organizations have joined [RTI's network]." However, we should have said, "According to RTI, more than 200 organizations have joined research programs that the DDS Technology Network complements."

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Integrators save with preconfigured subsystems

By Duncan Young

In general, an embeddable subsystem is a set of hardware and software modules working together to perform a specific function or set of functions needed by a specific platform or vehicle. Subsystems can be embedded within a larger system, for example an SBC plugged into a VPX (VITA 46) chassis, or a subsystem can be self-contained in its own chassis with a network or avionics interface connection to a larger system. Rugged SBCs are offered by many COTS vendors as "application ready" including preconfigured Built-In-Test (BIT) plus boot and recovery firmware and can be supplied with a preconfigured operating system such as VxWorks, Linux, or Windows with all the drivers needed to support the user's application. The procurement of SBCs using the vendor's specification and quality assurance systems is standard industry practice, but this concept has not been widely adopted at the higher level of an integrated chassis.

System integrator's perspective

To be successful, a system integrator must reduce risk, demonstrate a high state of technology readiness, and reduce time to deployment whether procuring a component, a COTS SBC, or a subsystem. Integrators are encouraged to use COTS products in as many platforms as possible, yet the perception is that the Technology Readiness Level (TRL) of board-level COTS products is relatively low as they still require integration, packaging, and verification to fit the requirements of their target applications.

Compatibility and interoperability

While COTS vendors make every reasonable effort to ensure that their products are designed to common specifications, it is impossible to test every combination of hardware, packaging, and software during initial design verification. With a typical vendor's product portfolio, this would lead to thousands of permutations for test. As a result, experience, best practice, and product life-cycle status are used to verify new designs. In some instances, to introduce an innovative concept, a standard might be adopted in an unusual way that is then not interoperable with every other similar product. An example of this is PMC/XMC, where power dissipation has grown from 15 W to 45 W, thus introducing special cases that can only become apparent in a small number of configurations. Similarly, VPX has encountered issues with control, data, and I/O plane allocations, prompting the introduction of OpenVPX (VITA 65) to create an assured level of system configurability.

Better business proposition

Chassis and power supplies also require configuration to allocate slots, interconnects, and external connections to suit an integrator's specific requirements. The resulting unique configuration must then be fully documented, environmentally characterized, and functionally tested. However, three key technology forces are changing this complex business proposition:

- PCI and PCI Express
- Network architectures
- SBC functionality and performance

PCI and PCI Express have introduced plug-and-play capability to system configuration; networks and Internet Protocol (IP) have revolutionized intra- and inter-subsystem communication. Finally, SBCs now have very high levels of performance and comprehensive application-oriented software support. A single SBC is well able to support even complex subsystems and, with the addition of PMC/XMC modules, can support a wide range of external I/O. The result is that many varieties of subsystems can be satisfied by a small number of variables in a chassis with only a few slots. This allows generic configuration, test, and characterization of a complete off-the-shelf, application-ready subsystem by the COTS vendor.

COTS subsystems

By reducing the variables, yet maintaining performance and functionality, a configured COTS subsystem is procurable off-the-shelf against its manufacturer's specification with a TRL significantly higher than those of its individual components. An example of this is the CRS range of two- or three-slot rugged subsystems from GE Intelligent Platforms, depicted in Figure 1. They are 3U CompactPCI-based, preconfigured with either Freescale MPC7448 or Intel Core SBCs with combinations of ARINC, MIL-STD-1553B, CANbus, DAC, ADC, network, and serial interfaces.

Figure 1 | A CRS rugged subsystem from GE Intelligent Platforms

Ideally suited to harsh environments, embedded computing applications in Unmanned Aerial Vehicles (UAVs), helicopters, small aircraft, and ground vehicles, an application-ready subsystem reduces risk and timescales to deployment for first- and second-tier systems integrators. In the future, further reductions in vital Size, Weight, and Power (SWaP) for these types of high-performance platforms can be anticipated, as the same principles of preconfiguration and verification are applied to, for example, newer architectures such as 3U VPX.

To learn more, e-mail Duncan at duncan_young1@sky.com.

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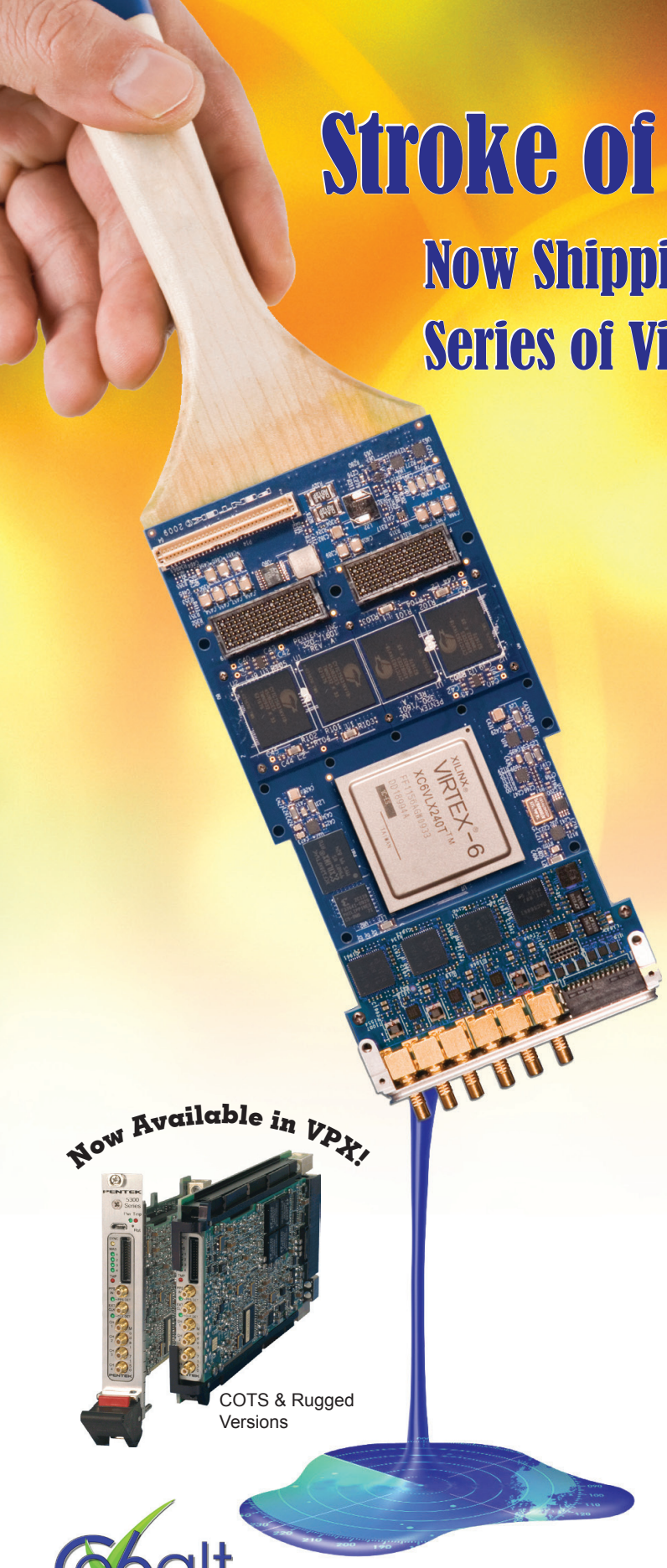

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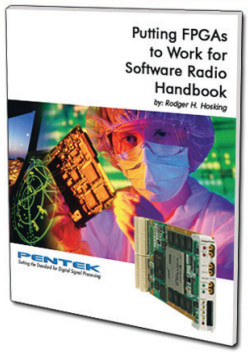

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Mil Tech Insider

AVX: A leap forward for DSP performance

By Steve Edwards

Intel's recent introduction of its Advanced Vector Extensions (AVX) represents a significant advance for improving calculation performance in DSP-processing applications. AVX doubles the vector registers' width from the 128-bit wide status quo provided by earlier vector extensions such as AltiVec, supported by Freescale's processors, and Intel's earlier Streaming SIMD Extensions (SSE). Intel first publicized AVX in March 2008 and launched it at the beginning of this year with the introduction of the second-generation Core i7 processors previously codenamed *Sandy Bridge.*

Doubling floating-point operations

Since the doubling to 256 bits, AVX registers can hold twice as many integer or floating-point values as the 128-bit AltiVec and SSE implementations. Vector extensions support integer calculation, but for DSP applications the important format is 32-bit single precision floating point. Floating point is the preferred fomat in military signal processing applications primarily because of the increased software development productivity as compared to the effort of managing the inevitable underflows and overflows of integer registers. AltiVec, first introduced with the PowerPC 7400, has always featured 128-bit registers, each of which could hold four "floats." The PPC 7400 processors, and later Intel processors with SSE, were able to perform eight simultaneous floating-point operations per clock cycle. By doubling the register size to 256 bits, AVX fits eight 32-bit values into each register, enabling 16 floating-point operations per cycle. This effectively, in one fell swoop, doubles the peak performance.

Putting AVX to work

The Fast Fourier Transform (FFT) is at the core of many DSP applications. Used to decompose periodic signals into their constituent sine waves, also known as *frequency bins*, the FFT is a *de facto* figure of merit to gauge processor performance.

How does AVX stack up to AltiVec and SSE? In application tests using VSIPL, the combination of AVX and a second-generation Intel Core i7 (2.1 GHz) processor did well when compared to AltiVec running on a Freescale 8640 (1 GHz) processor. Running a range of 1D complex FFTs with sample range sizes from 256 bytes to 512 Kbytes on a single core, the Intel/AVX platform's performance ranged 5 to 14x faster than the 8640. When compared on multiple 1D complex FFTs, the Intel/AVX platform measured 5 to 10x faster. When performance was compared running a complex matrix transpose, the Intel/AVX platform was rated at 7 to 26x faster. Also, in a test of vector multiply speed, the Intel/AVX was 4.6 to 72x faster than the 8640/AltiVec.

While some of this performance is coming from the faster clock of the Intel processor, these tests and others show that the AVX instruction set is contributing greatly to overall processor performance. Intel has published direct SSE versus AVX comparisons with benchmarks run on the same second-generation Core i7 processor with FFT performance improvements ranging from 1.2 to 1.8x. It is difficult to create a benchmark measuring pure AltiVec versus pure AVX because the amount of memory available to both types of processors differs. At the upper end of sample sizes, memory performance becomes more important, and the newer Core i7 features larger caches and higher memory bandwidth than are available to the 8640. These results underline the significance that doubling the raw performance of a floating-point machine holds for DSP applications. (For a copy of the test data, please contact the author.)

Curtiss-Wright Controls Embedded Computing (CWCEC) has several AVX-enabled products in development, including the DSP-oriented CHAMP-AV8 dual Core i7 board (Figure 1) aimed at leveraging this jump in performance.

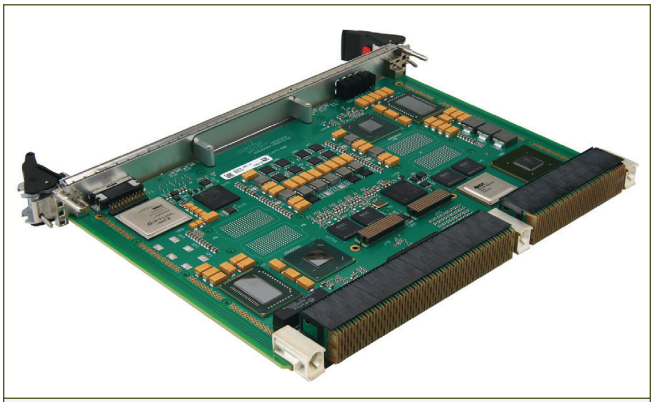

Figure 1 | The 6U OpenVPX CHAMP-AV8 from Curtiss-Wright Controls Embedded Computing features dual quad-core, second-generation Core i7 processors with 269 GFLOPS peak.

Changing the DSP performance landscape

While AltiVec, long the *de facto* standard for vector math calculation in military DSP platforms, changed the landscape for many years and enabled the use of general-purpose processors as an alternative to dedicated DSP chips, AVX is truly a significant upgrade. There might be greater improvements yet in store. When Intel upgraded the SSE instruction set for AVX, they rearchitected it and made it more easily extendable. This leaves the door open for easier transitions to even larger registers and keeps Intel's processors competitive as new alternatives for DSP – such as General Purpose Graphics Processing Units (GPGPUs) – begin to emerge.

To learn more, e-mail Steve at Steve.Edwards@curtisswright.com.

Legacy Software Migration

By Tim King

Migrating safety-critical software in military and aerospace systems

There are hundreds of millions of lines of legacy code in use in today's military and commercial avionics systems. Most of these legacy systems were developed using programming languages and development systems that are now obsolete (or obsolescing) and programming expertise that is no longer available. As a result, these legacy systems have become increasingly difficult and expensive to maintain and upgrade, thereby forcing developers to migrate their applications to new development hosts, compilers, safety-critical operating systems, and programming languages. In addition, the imposition of new standards and new requirements for certification from regulatory organizations can also trigger a need for software migration and reverification.

Migrating complex embedded software, specifically in applications requiring real-time response and a high degree of safety criticality, can be a costly, time consuming, and risky process requiring code changes, retesting, rereviewing, reanalyzing, and even recertifying. There are many factors that make legacy applications difficult to port. These factors include programming language nuances, compiler-specific implementations, runtime and hardware dependencies, the use of extensions beyond the defined programming language, and incompatible application code structures. Migrating applications can also impact reuse of code that has been certified to DO-178B or that will be certified to the upcoming DO-178C.

Migrating to a new language

The most challenging of all migration efforts is moving code written in a legacy language such as Ada or JOVIAL to another language such as C. Because the generated application will not be binary identical to the original, it will require at a minimum basic retesting and probably full reverification. Moreover, because the application must be modified at the source code level, new software engineers assigned to the program will likely have to be trained in the legacy programming language as well as in the application's design and inner workings. This will inevitably introduce bugs into the application. Other factors will also come into play. For example, the generated code will have a different layout and may no longer fit in the available memory. The data layout will also be different and no longer map correctly to the underlying hardware. Performance and timing aspects will also change.

> "... The bulk of DO-178B will remain intact, thereby simplifying the transition to DO-178C."

When changing languages, it is best to use a development environment that supports the legacy language as well as the new target language, with the ability to mix languages. This will allow designers to migrate slowly and to test in steps. While many compilers can combine code segments in different languages, most debugger tools handle only one language at a time. This means that developers must invoke several tools simultaneously to view interactions between code segments. These tools seldom interact in a coordinated fashion or exchange information to help correlate object code to multiple language sources. Mixed-language development environments such as DDC-I's OpenArbor allow mixed-language debugging from a single launch, making it easier to detect interaction errors and coordinate new and existing code.

Developers might also want to take advantage of tools and services that expedite the conversion process. These include semi-automated tools that convert applications in a predictable and straightforward manner while retaining the original application structure and source code comments. This enables the converted code to be readable and maintainable, minimizes the risk of introducing software errors, and eliminates any further dependency on the software conversion tool. Once in the new language, the application can then be optimized with newer language features and/or augmented with new functionality.

DO-178B/DO-178C migration

If an application was originally certified to DO-178B and it is migrated, it will have to be reverified and recertified with the new language, development environment, verification environment, and runtime environment. As mentioned, later this year, the industry will begin its transition from DO-178B to DO-178C, which will have new implications, both in new development and legacy code reuse. Along with adding some clarification to the guidance of DO-178B, the DO-178C document adds new guidance to accommodate development technologies that have become common since the publication of DO-178B, including object-oriented programming, model-based development (UML or Simulink), tool qualification, and formal methods.

The good news for developers is that DO-178C preserves the core DO-178B guidance with some modifications for clarification. Developers will still have to familiarize themselves with the guidance in each area applicable to their specific processes and procedures. Developers will also have to assess the impact of the additional guidance, tailor their processes and procedures accordingly, and update any software and certification artifacts that they migrate. However, the bulk of DO-178B will remain intact, thereby simplifying the transition to DO-178C.

***Tim King** is Technical Marketing Manager at DDC-I. He can be contacted at tking@ddci.com.*

Daily Briefing: News Snippets

By Sharon Hess, Assistant Managing Editor

www.mil-embedded.com/dailybriefing

SECDEF Gates to step down

After what appears to be one of the most noteworthy stints as defense secretary, Robert M. Gates is calling it quits. Starting retirement at the end of June, Gates' move will effectively end the Gates/Obama defense era, which included too many jaw-dropping announcements to restate here (all but the first increment of FCS, the F-22, and USJFCOM, to name a few). As we went to press, President Obama is expected to nominate Leon Panetta, CIA Director, for SECDEF, and International Security Assistance Force Commander/U.S. Forces-Afghanistan Commander Army Gen. David H. Petraeus (Figure 1) will be nominated to step into Panetta's former office, according to a Pentagon senior administration official. What remains to be seen is 1) whether the Senate will confirm the Panetta nomination; 2) what effect this round of White House musical chairs will have on national security; and 3) what the Obama/Panetta era holds for the defense industry. (For more information on the proposed 2012 defense budget, visit www.defense.gov/news/newsarticle.aspx?id=62803.)

Figure 1 | The end of an era: SECDEF Robert M. Gates (pictured) calls it a day, retiring from his post effective June 30. Meanwhile, as we went to press, a senior Pentagon administration official says Pres Obama will nominate Leon Panetta, CIA Director, as Gates' successor, with Gen. David H. Petraeus (pictured) then filling Panetta's shoes. DoD photo by Cherie Cullen

PAF to get linked in to Link 16

The Pakistan Air Force (PAF) is about to gain more advanced comms and training abilities, thanks to a recent fourth USAF Electronic Systems Center (ESC) order for a Link 16 tactical Ground Support System (GSS), which will be provided by Tactical Communications Group (TCG) and used by PAF. The GSS is COTS based and touted to provide Link 16 situational awareness and simulation training that can be utilized on F-16s owned by PAF. Specifically, PAF can conduct Link 16 aviation and network personnel training, with the bonus of possible future add-on data link networking capabilities. The purchased GSS is an expanded version of TCG's Ground Tactical Data Link System (GTS). The GSS first goes to the U.S. government, then TCG installs and tests it in Pakistan, where it will be implemented with unannounced "requested optional features," TCG reports.

USMC warns with NL/TLMS

Many or most military technologies are lethal, but the USMC recently contracted with Combined Systems, Inc. (CSI) to make and deliver a nicer type of munition: a quantity of 225 three-bank, 40 mm Non-Lethal/Tube Launched Munitions Systems (NL/TLMS). The NL/TLMS can fire 30 rounds of flash-bang, non-lethal munitions, and, under the $11 million contract, CSI additionally will fabricate, produce, and ship 75,000 munitions rounds, along with spares, training, and contractor logistics support for up to two years. NL/TLMS is designed to spew non-lethal fire at high volumes to increase soldier safety in convoy security operations and at entry control points and vehicle check points. Work is slated for completion in April 2012, and contract options could increase the total contract value to $13 million.

RAAF C-17's aid Japan and others

The Royal Australian Air Force (RAAF) has really put its C-17 (Figure 2) fleet through its paces recently. The Aussie-owned C-17 Globemaster III's sojourned to Japan to render relief to areas affected by the recent tsunami and earthquake, as part of Operation Pacific Assist. The airlifters were used to transport more than 1 million lbs of vehicles, food and water, cooling pumps for the Fukushima nuclear plant, and various disaster relief equipment. Prior to that, C-17's helped RAAF provide aid to earthquake-torn areas in Christchurch, New Zealand, in addition to communities ravaged by floods in Queensland, Australia. With all that C-17-proving experience under its belt, the RAAF recently approached the USAF with an immediate-need request to add C-17 No. 5 to its fleet. The USAF approved the Foreign Military Sale, and the Boeing-incarnated C-17 will join the RAAF this August, to be used by RAAF Base Amberley's 36 Squadron, housed close to Brisbane.

Figure 2 | Royal Australian Air Force (RAAF) C-17 Globemaster III's recently traveled far and near, rendering disaster relief in Japan, New Zealand, and nearby Queensland, Australia. Subsequently, the RAAF ordered one more immediate-need C-17, to be delivered this August. Boeing photo

Aegis combat systems pass the test

The Aegis combat system climbed aboard (with aid of Lockheed Martin's Aegis team and the U.S. Navy) two Navy guided-missile destroyers – the USS Jason Dunham (DDG 109) and the USS Gravely (DDG 107 – see Figure 3). Aegis' mission (for the time being): To undergo thorough anti-air, subsurface, and surface warfare exercises as part of Aegis' recent Combat Systems Ship Qualification Trials. The trials included air defense and tactical data link testing, along with electronic attack and manned raid situations. The outcome: *fait accompli* – Aegis was certified "fully operational." The recently tested Aegis is the combat system's 15th evolution. And, when suited up with the vertical launching system dubbed "MK 41," Aegis can handle any type of naval-warfare threat environment or mission. The USS Jason Dunham and USS Gravely are categorized as Arleigh Burke-class destroyers.

Figure 3 | The USS Jason Dunham and USS Gravely Navy destroyers were recently fitted with the 15th evolution of the Aegis combat system – which was certified as fully operational. Pictured: the USS Gravely, named after the late Vice Adm. Samuel L. Gravely Jr., the first African American to command a warship. U.S. Navy photo courtesy of Northrop Grumman

Mergers and acquisitions

One thing that never stops in the defense realm is Merger and Acquisition Row (Figure 4). Some of the recent shuffles included: **Curtiss-Wright Flow Control Company** acquired aviation support vehicles supplier **Douglas Equipment Ltd.** for $20 million (cash) in April. Also in April, **M/A-COM Technology Solutions,** a supplier of high-performance semiconductors and subassemblies for RF/microwave, acquired (for an unknown sum) **Optomai, Inc.,** a fabless semiconductor company developing ICs for 40/100 Gbps fiber-optic. The month of April also saw **ENSCO, Inc.'s IData Visual Systems** subsidiary – which supplies technology, science, and engineering for A&D – acquire **Quantum3D's IData and IGL 178 product lines** for an undisclosed sum. And finally, May's showers brought acquisition flowers: Mission-critical development tool/runtime environment provider **Atego** acquired **HighRely**, a DO-254/DO-178B engineering services provider, at an unannounced purchase price.

ACQUIRER	WHO/WHAT ACQUIRED	AMOUNT
Curtiss-Wright Flow Control Company	Douglas Equipment Ltd.	$20 million (cash)
M/A-COM Technology Solutions	Optomai, Inc.	Unknown
IData Visual Systems	Quantum3D's IData and IGL 178 product lines	Unknown
Atego	HighRely	Unknown

Figure 4 | A summary of recent industry-acquisition activity.

Figure 5 | Some 3,034 of the U.S. Army's Bradley Fighting Vehicles will soon be fitted with BUSK III survivability kits per a recent U.S. Army/BAE Systems contract. U.S. Army photo by Spc. Khori D. Johnson, 3/4 AAB PAO

Bradley vehicles: Armed and (less) dangerous?

Battlefield survivability is priority No. 1, and a recent contract between BAE Systems and the U.S. Army makes this mantra a reality. Specifically, the $53 million contract stipulates that BAE renders 3,034 of its Bradley Urban Survivability Kits (BUSK) III, which provide deployed Bradley Fighting Vehicles (and therefore the soldiers who ride in them) with enhanced survivability (Figure 5). Said enhancements include: 1) Emergency Ramp Release for emergency egress for vehicles damaged in theater; 2) Bradley Fuel Cell Survivability, providing a lower fuel cell bladder to increase fuel containment as IED situations occur; 3) Bradley Advanced Survivability Seats-Driver, proffering foot rests and seats that absorb energy and lower vehicle-floor-emitted blast effects; and 4) a Turret Advanced Survivability System comprises floor plates and foot rests for commander/gunner positions for extra safety during IED events. Busk III constitutes the third iteration of BUSK survivability enhancements, and contract work is slated for completion on June 30, 2011.

UH-60/AH-64 helicopters get an overhaul

The venerable AH-64 and UH-60 Black Hawk (Figure 6) helicopters, in U.S. Army service since 1984 and 1979, respectively, are about to get an overhaul per a recent $17 million contract with General Electric Engine Services, Inc. The contract specifies that GE provides turbine engine cold section modules – 120 T700-GE-701C/D and 30 T700-GE0700 modules – for overhauling AH-64 Apache and UH-60 Black Hawk helicopters. Work will occur by March 2015 in Arkansas City, KS. The contracting activity is the U.S. Army Contracting Command located in Redstone Arsenal, Alabama.

Figure 6 | General Electric Engine Services, Inc. will provide the U.S. Army with 150 turbine engine cold section modules for UH-60 Black Hawk (pictured) and AH-64 Apache helicopters. U.S. Army photo by Staff Sgt. Jason Epperson, 3rd MEB PAO

The iPad factor: Preparing for the commoditization of military embedded Virtual Training Simulation devices

By Andy Morris

The next generation of embedded devices might be less a result of government and industry-led R&D efforts than ever before. These new, consumer-oriented systems will be based on today's tablets, smartphones, and gaming toolkits, offering compelling price points and performance characteristics. This will make it increasingly difficult to justify custom hardware systems and technologies for applications such as aircraft and ground vehicle Multi-Function Displays (MFDs), or even proprietary handheld devices. Rather than viewing this shift as a disruptive force, there are specific practices developers and integrators of embedded military systems can take to make the most of this coming sea change in the industry, which is already occurring in the military's Virtual Training Simulation (VTS) realm.

U.S. Army photo by C. Todd Lopez

Turnkey embedded military systems today offer extensive integration options and combat-tested performance. However, the typical closed-system approach can limit the full potential of these devices. Recent advances in smartphones, tablets, and gaming tookit software and hardware technology now deliver visual fidelity and performance previously limited to desktop PCs. Imagine a pilot being able to troubleshoot an in-flight emergency, like a landing gear deployment problem, with the same visual troubleshooting procedure presented in classroom training. This capability is available today for those who choose to invest in the new generation of Virtual Training Simulation (VTS) tools and techniques.

There are two primary factors driving development in VTS for embedded military systems: the commoditization of high-performance graphics on mobile devices, and royalty-free or open-source game toolkits. As an example, the U.S. Army is testing the Joint Battle Command-Platform smartphone based on Google's free Android operating system for field operations, including platoon location via GPS. And the open-source Delta3D engine was used to prototype the Nemesis game-based-learning application, with an objective to train operators in the decision-making and psycho-motor skills required for the U.S. Army Humanitarian Demining Program.

The Army's Connecting Soldiers to Digital Applications (CSDA) program is also sponsoring the development of mobile simulation applications. Miniaturization and economies of scale have brought affordable realism to tablets, while leading game toolkits now allow developers to deploy the same source code from dedicated game consoles down to Android and Apple iOS

devices. Agile organizations will continue to take advantage of both hardware and software advances in the tablet/smartphone and game toolkit realms to quickly and affordably build highly deployable solutions.

The tablet as a Just-In-Time (JIT) training platform

With fast, dual-core CPUs and independent graphics processors, the current generation of tablets enables the simulation of highly complex and detailed procedures, such as diagnosing fault codes from an onboard weapons system to determine the appropriate tools and techniques required for repair. The original Apple iPad included a single 1 GHz A4 processor and a PowerVR SGX 535 Graphics Processing Unit (GPU). This was indeed a powerful first-generation offering, but limited therealism of training simulations by reducing the speed of draw-calls far beneath graphics cards found on entry-level PCs. The iPad 2 now contains a dual-core 1 GHz Apple A5 processor (see Figure 1) as well as updated dual-core

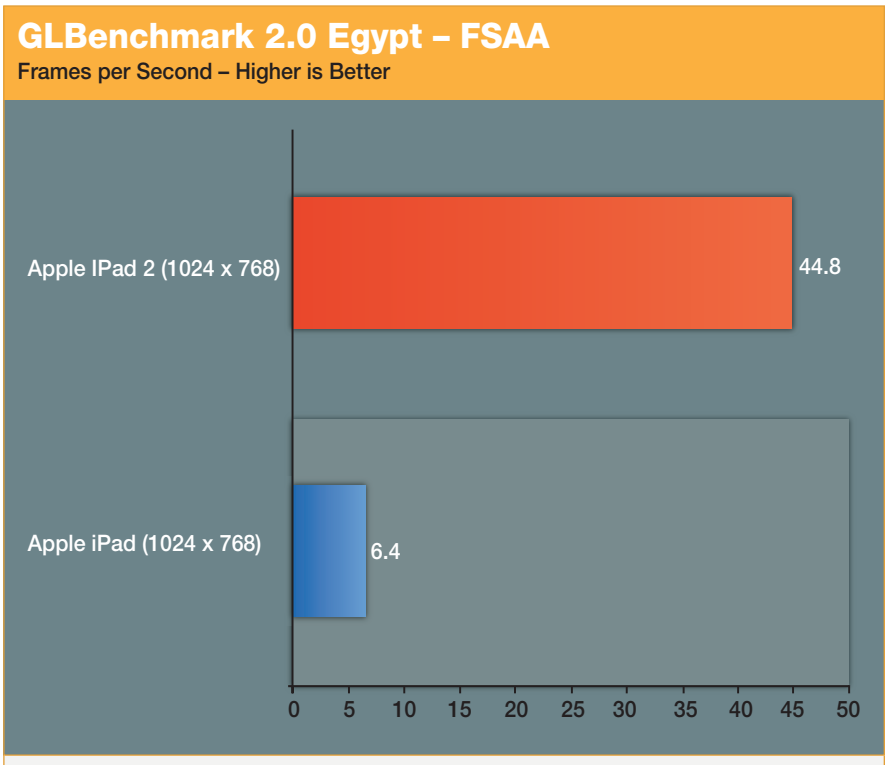

Figure 1 | Original iPad versus iPad 2 GLBenchmark 2.0. iPad 2 allows for 3D performance up to nine times faster. Data courtesy of AnandTech.com

PowerVR SGX543MP2 graphics. This allows for 3D performance up to nine times faster[1]. Technology research firm AnandTech.com found a more modest but still impressive range of 3 to 7x in GLBenchmark 2.0 improvement over the original iPad, running games that had yet to be optimized for the enhanced iPad 2 capabilities[2]. And the expansion of graphics powerhouse NVIDIA into the mobile market promises to maintain healthy price and performance competition in the market.

Complex maintenance and troubleshooting procedures that were recently limited to paper can now be rendered effectively on a compact display. Even laptops are being made obsolete, or at least presented with a compelling trade off, by these new ultra-portable computers that offer near-laptop performance for a fraction of the size and weight. And a networked tablet turns an Interactive Electronic Technical Manual (IETM) into a document that can be updated with the latest technical updates wherever the warfighter needs operational support. High-resolution displays (up to 960 x 640 pixels) make mobile simulation a possibility on once unthinkably small screens like the 3.2-inch diagonally HTC Aria or the 16:9 aspect ratio Motorola Droid. And standards bodies such as S1000D and DITA remain vested in making sure that their documents are accepted by procurers of embedded military systems.

> “High-resolution displays (up to 960 x 640 pixels) make mobile simulation a possibility on once unthinkably small screens like the 3.2-inch diagonally HTC Aria or the 16:9 aspect ratio Motorola Droid.”

Game toolkits enable software advances

Toolkit providers now recognize the opportunity to broaden the customer base for development beyond recreational gaming. A driving factor is the Armed Forces' adoption of virtual training and simulation as key tools for increasing training capability and capacity, while lowering training costs and hazards associated with live training. According to research from Visiongain, global spending in 2009 on military simulation and virtual training reached $8.4 billion, and will continue to increase through 2020[3].

As promising as commercial tablet development is to embedded military

Figure 2 | Interactive Patriot Missile training on the Apple iPad

systems, recent developments in software are even more compelling. The commercial video game industry is responsible for driving DirectX and OpenGL graphics performance on PCs. The defense industry recognized this fact several years ago, and has been leveraging the same powerful toolkits to build "Serious Games" (SGs) such as America's Army and simulation-based training. However, until recently these toolkits suffered from significant disincentives: They cost hundreds of thousands of dollars or incurred large royalty payments, and development had to be targeted to one specific platform such as a PC game console.

Now, a developer can produce VTSs for PC instructor-led training, and deploy the same code base to an embedded military mobile device running Android or Apple iOS for little or no additional cost. This approach is opening up game toolkits to hundreds of new developers, many of whom contribute valuable input that serves to improve the performance and feature set. Expanded capabilities, such as the bundling of expensive physics libraries, bring even more developers onboard who continue to push the envelope and pioneer new use cases in a virtuous circle.

One example is a commercial game toolkit adopted to demonstrate a military training concept: The company created a VTS prototype that requires users to perform a routine maintenance task from a first-person perspective. Individual steps within the maintenance trainer require learners to open hatches, move levers, toggle dials, and use a grounding tool. Whenever learners miss a step or perform a step out of order, a warning appears, explaining the error and its consequences. This critical-path training approach ensures that learners master proper operations and maintenance procedures before working with actual military equipment. Once the learners complete the maintenance task, a series of questions provides a measurable check-for-understanding.

This application was developed by Heartwood in collaboration with Unity 3D, and Raytheon leveraged this unique software technology when it selected Heartwood to develop a fully immersive 3D maintenance training program for the Patriot Air and Missile Defense System's radar set (Figure 2). After a PC version was completed, the client requested a Web-enabled method of user access, which resulted in a full Web-enabled virtual training program. These applications are now being deployed to the Apple iPad, using the same Unity 3D code base but optimized for JIT or refresher training. Additional optimization was required, but the core functionality remains intact as well as the original 3D models, simulation, and logic. Carrying the evolution another step forward, these fully mobile versions of the application aim to deliver the ultimate promise of embedded military systems: sustainable, on-demand decision support.

Transforming commoditization into strategic advantage

Advances in tablet computing, smartphones, and game development have the ability to transform embedded military systems. Additionally, off-the-shelf hardware and low-cost toolkits make VTS a reality in an aircraft cockpit, ground vehicle MFD, or anywhere the warfighter needs to make the right decision the first time. Prototypes can be built quickly and effectively to determine whether the cost and performance advantages merit supplementing or replacing existing embedded technologies.

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Static analysis is going deeper with deep-flow data flow

Interview with Jill Britton, Consultancy Services Group Manager at PRQA

U.S. Air Force Photo/Staff Sgt. Eric Harris

EDITOR'S NOTE

In the past 12 months, I've interviewed most of the major static analysis companies and can spot the similarities between their approaches. But in this interview with Jill Britton from PRQA, she tosses out a new-to-me term: "deep-flow data analysis." Read on to see how it differs from (or is similar to) other static analysis tools you may be familiar with. Edited excerpts follow. – Chris A. Ciufo, Editor

MIL EMBEDDED: ***Let's start with an overview of what PRQA does, please.***

BRITTON: We [primarily] work with static analysis of C and C++ and are particularly interested in coding standards compliance. We've been working in this area for more than 20 years. We're a committee member of MISRA and a committee member for ISO C. We have offices in the U.K., U.S., Netherlands, and India. We also have distribution partners in the Far East and Germany. Our main products are QA-C, QA-C++. We have compliance modules for MISRA, JSF, and high-integrity C++, which is our own product and freely distributed. We have partnerships with products such as VectorCAST for dynamic analysis and S101. We also provide services such as customer coding standards reviews, code audits, and general integration of our products into customers' own build systems.

MIL EMBEDDED: ***You said compliance with JSF – what is JSF?***

BRITTON: JSF is the Joint Strike Fighter and it has a C++ aeronautical coding standard. As MISRA is to cars, JSF is to the [defense] aeronautical industry.

MIL EMBEDDED: ***Tell me what is new in the software industry and where your products fit in.***

BRITTON: The biggest thing in all the embedded industries is the rapid increase in lines of code. Ten years ago, you had thousands of lines of code; it's now into the hundreds of thousands of lines of code. Critical safety issues are paramount. It's very important that all software is tested and is as "safe" as possible, which is why you would have the coding standard. Our tool allows you to check the basic problems of code before it goes into test, so that major issues are avoided. The static analysis takes the code from the engineer completely and runs through it to check for obvious errors and undefined behavior. It replaces some types of peer review and adds an extra level of confidence to the code.

> "Relative to legacy code within the military environment, there's often an attitude of 'If it isn't broken, don't fix it.'"

MIL EMBEDDED: ***What are the key methodologies for code analysis?***

BRITTON: Well one of the new things that is coming to [our tool] is a deep-flow data flow analysis, which takes us into a deeper level of understanding of the code and highlights problems that arise in their own right or are associated with other bugs in design and coding, for example, uninitialized data (attempting to use a variable without setting a value to it) and array-bound violations (allowing data beyond the range of the array). These can cause some difficult-to-detect bugs. This data-flow analysis is a very powerful technique and is going to be in our new release of QA-C.

MIL EMBEDDED: ***Is "deep-flow data flow analysis" an industry term and you're just now implementing it?***

BRITTON: "Data flow analysis" is not our propriety name. It's an industry name. But "deep-flow data flow analysis" is a term we use ourselves, and it comes from doing analysis on the static code to get the flow of the data through.

Our strength is our coding standards. We work from the point of view of educating the user into best practice, rather than merely pointing out bugs. We have an extensive help system that shows the user why one of these messages or errors has come up. Our in-depth knowledge comes from an extensive understanding of the language itself rather than just the code.

MIL EMBEDDED: ***How do you compare to, say, Coverity or LDRA?***

BRITTON: Again, it's the static code – we concentrate on being excellent at the static code analysis. And for dynamic analysis, we partner with VectorCAST so that we can both bring in what we're good at.

MIL EMBEDDED: ***What is the difference between static analysis and dynamic analysis?***

BRITTON: Well, the dynamic is more about the behavior of the code during execution, actually *running* the code. Static analysis is performed without running the code but identifies code that is potentially dangerous, overly complex, or difficult to maintain. For PRQA, again, it's the fact that we look at the language and the constructs of the language rather than what happens when you put data in. Our tool works in a very similar way to the compiler itself, in that it preprocesses the source and can detect things such as infinite loops, signed integer flows, and so on. We also have this deep-flow data flow, which although it is not the same as our competitors, it is using some of the aspects that they use as well.

MIL EMBEDDED: ***What are some of the common coding errors that are difficult or impossible to detect?***

BRITTON: Well, one is the infinite loop. An infinite loop might be intentional – perhaps if you have a while (1) loop or something you want to just continuously run in a particular task – but it also might not be intentional. Another one is signed integer overflow, which can lead to things such as divide by zero, causing the code to just not execute as expected.

Another thing not necessarily obvious is that the compiler is not infallible. Within our static analysis tool, we can find code errors that the compiler allowed through. This is where we come into the type checking, leading to the possible signed integer overflows and type misuses.

MIL EMBEDDED: ***Let's talk about defense systems. How do defense applications differ from other applications?***

BRITTON: There are three key issues. Firstly, the safety-critical aspect is very important with defense applications. Secondly, the timescale used on military projects is often much longer than any other embedded-type systems. For example, an automotive product might be on the market within two years, whereas military projects might be five or longer. So there is maybe a slower adoption of changes. And finally, there's the whole issue of using legacy code.

MIL EMBEDDED: ***Let's talk about each of these three scenarios you've described – safety-critical code and more use of legacy software combined with longer timescale.***

BRITTON: For safety-critical systems, software must be reliable, tested, and infallible in the field. There are many ways of addressing this. One important thing is the process that is gone through [certification testing] before the code is released, like DO-178B. PRQA's tools are qualified for use in DO-178B. DO-178C is coming out shortly, which is enhancing this field again. Static analysis is a very important part of this because it can remove problems before even getting to test and reduces the testing cycle, allowing concentration on more detailed and definite testing.

Relative to legacy code within the military environment, there's often an attitude of "If it isn't broken, don't fix it." The legacy code doesn't undergo as rigorous standards testing as new code does – purely because standards didn't exist when it was created; however, it can pretty much be taken onboard that the legacy code that has been in a product maybe for 20 years is reasonably likely to be safe.

MIL EMBEDDED: ***So what happens to the legacy code as far as static analysis goes?***

BRITTON: So, with our static analysis tool we will exclude that code from the analysis on the basis that you may cause more trouble by making changes to that code than in actually fixing anything that's found. We call this "baselining": We take a snapshot and say, "From this point onward, anything new that goes in will be checked to this coding standard." Obviously, legacy code can be brought in step by step. Very often this isn't done purely because the working code that's been safely used for several years, you don't change. Traceability is always very, very important, too.

MIL EMBEDDED: ***Is this baselining you mentioned unique to your tool? Are we talking about 20-year-old C code or Pascal?***

BRITTON: With this kind of concept, different companies call it different names. We only analyze C and C++, so if it's Pascal code, we wouldn't analyze it. We see a lot of C in military products, more than C++, although C++ is increasing in that world. With legacy code, if you want to go in and clean it up, the baseline can be moved back and allow more code to be changed. This can be risky and is not a particularly useful exercise.

MIL EMBEDDED: ***Some big trends in defense are multicore, partitioned RTOSs, and virtualization. How have these affected coding practices, and how do tools manage them?***

BRITTON: We have dealt with multicore systems and we are currently working on improvements to the system working with multicore. Certainly, regarding the partitioned OS, our product basically runs where you put it and takes the code as presented to it. The whole goal – all the new trends, virtualization, everything – is to head toward safer, speedier, and easier-to-understand, top-level systems.

MIL EMBEDDED: ***Let's polish the crystal ball: Which trends do you see going forward?***

BRITTON: Well, I think there will be more software, more lines of code, more standards, and developments in language. Particularly in some of the U.S. universities, there's a lot of interesting work going on with new programming languages that may be used in future embedded applications. Another trend is the cloud. I'm not sure how that will affect the embedded world, but it needs to be considered. And finally, I think there will be a transfer to more object-oriented languages using C++, rather than C.

Jill Britton, *Consultancy Services Group Manager at PRQA, has 30 years of embedded software experience in a variety of areas including defense, automotive, telecommunications, and education. She spent 12 years working at Motorola, designing software for both network devices and automotive applications. She has also worked on telematics for Continental Automotive.*

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U.S. Marine Corps photo by Lance Cpl. Orlando Perez

Serial RapidIO with Intel-based DSP embedded systems saves slots and boosts performance

By Ian Stalker and Devashish Paul

Until now, it was not possible for x86 DSP system designers to harness native Serial RapidIO support. However, the 2nd-Gen Intel Core i7 processor, along with PCIe2-to-SerialRapidIO2 bridging technology, is bringing high performance to military-use DSP engines.

Serial RapidIO is well established as the switched serial fabric of choice for high-performance Digital Signal Processing (DSP) in embedded military applications. Its use is well defined and supported by the OpenVPX/VITA 65 standard. But until recently, Serial RapidIO has only been practical for use in Power Architecture-based systems. Thanks to the recent introduction of Intel's 2nd-Generation Core i7-2715QE quad-core processor, and a PCI Express-to-Serial RapidIO bridge, x86-based embedded military DSPs are now able to take full advantage of the Serial RapidIO interconnect for DSP processing. The new Core i7 features the numerous improvements of the Intel Sandy Bridge architecture aimed at performance and efficiency. And it offers 256-bit wide Advanced Vector Extensions (AVX) floating-point instructions that effectively double the peak floating-point performance compared with the previous 128-bit SSE instructions that form the core of fundamental DSP calculations such as Fast Fourier Transforms (FFTs).

Prior to this latest generation of Core i7, there had been no practical support for Serial RapidIO using Intel processors. This greatly limited the viability of the Intel architecture's use in military and aerospace DSP multiprocessor systems. Attempts at doing PCIe-to-Serial RapidIO protocol conversion in FPGAs were expensive and lacked the Serial RapidIO messaging support that is so useful for control loops in signal processing applications. Alternately, fabric solutions for Intel architecture-based distributed systems included InfiniBand, which is used in the enterprise computing world but is not preferred by military system integrators. Another choice is Gigabit Ethernet. For single board computers, where the requirement is typically a single processor communicating with I/O, these interconnect choices have been sufficient. However, due to lack of native Serial RapidIO support, system designers either could not use Intel-based processors, or if they wanted to use Intel-based architectures, had performance limitations because they were unable to use Serial RapidIO as their data plane interconnect.

The good news is that the Intel Core i7 Gen2 combined with a new generation of PCI Express (PCIe) Gen2-to-Serial RapidIO Gen2 bridge provides a solution for direct Serial RapidIO support on Intel-based platforms. The following discussion provides a comparison of Serial RapidIO to 10 GbE in DSP systems as well as a look at this enabling bridge technology.

10 GbE versus Serial RapidIO

In comparing Serial RapidIO to 10 GbE, the short answer is that Serial RapidIO provides significantly higher performance and saves valuable board slots compared to 10 GbE implementations

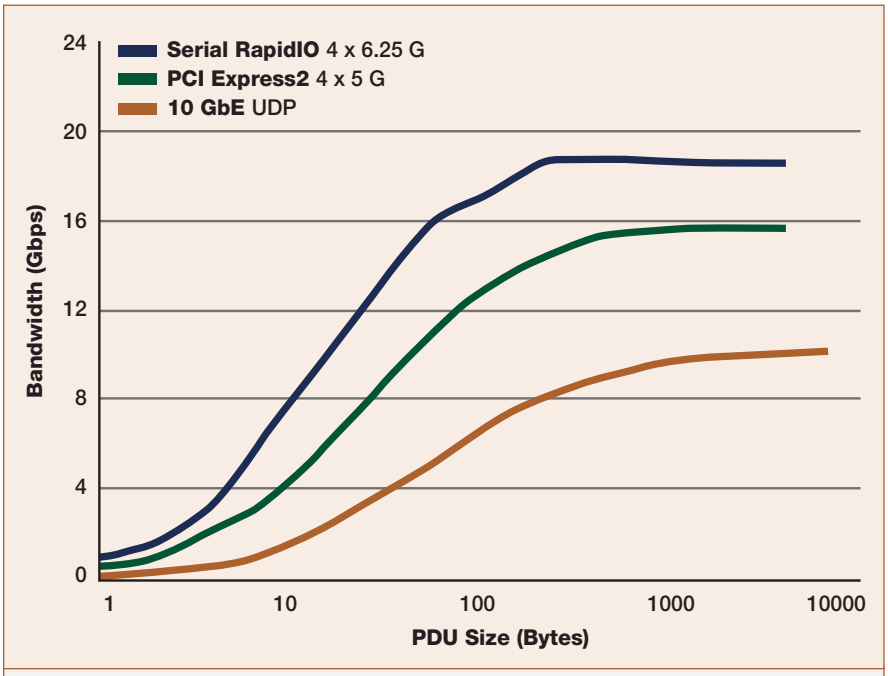

Figure 1 | A comparison of Serial RapidIO, PCI Express2, and 10 GbE

(Figure 1). Furthermore, Serial RapidIO supports distributed switch architectures, and Serial RapidIO switches are small, low-power devices (starting at 21 mm x 21 mm, ~3 W). Their size and functionality make it common for board designers to provide a Serial RapidIO switch onboard their DSP engine cards to locally aggregate multiple computing nodes. While it's theoretically possible to build DSP boards that have an Ethernet switch onboard, Ethernet switches are significantly larger (typically 30 mm x 30 mm to 40 mm x 40 mm and no small lane count options) than Serial RapidIO Gen2 switches, which are available in 16- and 32-lane options. On a practical level, these bigger, power hungry devices, built for use in the enterprise/IT environment, are too cumbersome to deploy onboard a 3U or 6U VPX multiprocessor DSP engine. Where Ethernet switches are used in DSP applications today, they require a separate card, taking up valuable slot space and adding weight (a typical rugged card weighs 1.0-1.2 Kg) in SWaP-constrained military platforms. For systems that require a high level of fault tolerance, designers must add a second redundant Ethernet switch, consuming an additional slot and adding even more weight.

Additionally, Ethernet switches offer end-to-end packet termination latency that can be in the order of milliseconds and also require processor intervention to terminate the protocol stack. This results in major performance and overall system power penalties that make it a nonstarter for real-time military and aerospace systems that are rack-space, power-consumption, and cooling-capacity constrained.

Moreover, 10 GbE is not ideal for supporting all of the system topologies that Serial RapidIO can easily support. The majority of embedded DSP systems deployed today are fewer than eight slots. One of the common topologies used on these distributed processing systems is a full-mesh architecture in which each card is connected to every other card. This approach is attractive because it delivers very high card-to-card bandwidth and does not exhibit a single point of failure. OpenVPX defines four ports on the data plane. A system designer can use these four ports to build five-card distributed systems in which each card has a connection to the other four. While the five-card full-mesh is the ultimate in card-to-card bandwidth, larger systems can also be constructed using distributed switching where packets pass through the switches of intermediate cards. The high bandwidth of Serial RapidIO makes this practical for systems up to 16 slots in size.

A typical Intel-based DSP system using 10 GbE would require at least six slots, with one for a dedicated Ethernet switch card. This is compared to the five slots required in a system using Serial RapidIO, as each DSP card can have multiple bridges per processor, mapped into a small Serial RapidIO switch and then have 4x4 Serial RapidIO links to the backplane. This reduction in system slots delivers benefits far beyond familiar Size, Weight, and Power (SWaP) hurdles. Minimizing the board count will improve Mean Time Between Failures (MTBF).

Another aspect of DSP system design where Serial RapidIO-based boards provide an advantage over 10 GbE is in hybrid-processor/FPGA designs. Virtually every new system design today includes a mix of FPGAs and conventional microprocessors. Implementing Serial RapidIO in an FPGA is more practical than adding 10 GbE into an FPGA. That's because terminating 10 GbE requires an additional processor (and software) and can't be done autonomously in FPGA code.

PCIe2-to-Serial RapidIO2 protocol conversion bridge

The goal of military DSP systems designed for use in signal processing applications is optimal bandwidth and reliability in rugged environments. To deliver the near real-time processing of analog sensor data needed to identify signals of interest requires the best achievable combination of data throughput and low latency. In today's embedded system design environment, that combination is best delivered with the joint solution consisting of the Core i7 and rugged DSP engines based on a PCI Express (PCIe) Gen2-to-Serial RapidIO Gen2 bridge, versus a 10 GbE path.

These bridges can provide mapping from PCIe Gen2 into a Serial RapidIO Gen2-based switch onboard and into the backplane. The bridges can be as small as 13 mm x 13 mm, and support memory mapped transfers and Serial RapidIO messaging. PCIe Gen2-to-SerialRapidIO2 bridges can deliver 16 Gbps, compared to 10 Gbps supported by 10 GbE. The performance of 10 GbE drops even further when packet sizes are small, which is the preferred approach in embedded systems for better real-time performance. For 256-byte packets, 10 GbE delivers only 8 Gbps throughput.

IDT's Tsi721 is an example of such a PCIe Gen2-to-SerialRapidIO2 bridge, and makes any processor look like a PowerPC to the Serial RapidIO network. A key feature is that each of the bridge's

8 DMA and 8 messaging transmit and receive queues is able to support the full 16 Gbps line rate for 64 byte and larger packets. These features make it possible to transfer large amounts of data in a DSP system with low latency at 16 Gbps. Thus, a given channel can be mapped to a physical core in a processor, or even a virtual context, maximizing performance at a system level and simplifying system software development.

Figure 2 depicts a rugged, high-performance DSP engine that harnesses the combination of Serial RapidIO and Intel's latest Core i7: the new OpenVPX CHAMP-AV8 from Curtiss-Wright Controls Embedded Computing. The dual Core i7 card, DSP engine utilizes IDT's Tsi721 bridge. CHAMP-AV8's processors deliver up to 269 GFLOPS. With IDT's bridge chip, the card delivers triple the bandwidth of first-generation VPX products (up to 160 Gbps fabric performance). This once again proves that Serial RapidIO is a high-performance path to DSP system implementation.

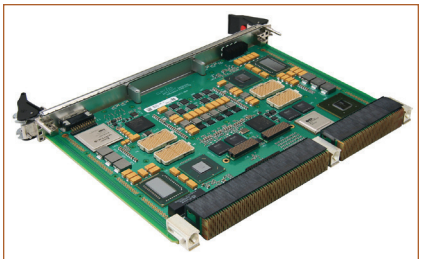

Figure 2 | The CHAMP-AV8 dual Core i7 card, DSP engine utilizes IDT's Tsi721 bridge in addition to Serial RapidIO and Intel's latest Core i7.

Editor's note: *Curtiss-Wright Controls has two separate and distinct divisions working on embedded technologies. This article was written by CWCEC (Curtiss-Wright Controls Embedded Computing).*

Ian Stalker *is the DSP Product Manager for Curtiss-Wright Controls Embedded Computing. He has more than 20 years of experience in the embedded industry and holds a degree in Electronics Engineering. Contact him at ian.stalker@curtisswright.com.*

Curtiss-Wright Controls Embedded Computing
703-779-7800
www.cwcembedded.com

Devashish Paul *is a Senior Product Manager for Serial RapidIO at IDT. In the past 15 years, he has run several product lines for Tundra and IDT, focused on embedded interconnect and network processing. Before that, he served in the Canadian Air Force as a systems engineer for the CP-140 and the F-18 programs, achieving the rank of Capt. He holds a Bachelor's degree in Electrical Engineering from the Royal Military College of Canada, as well as a Masters in Electrical Engineering in Digital Signal Processing and an MBA from the University of Ottawa. Email him at Devashish.Paul@idt.com.*

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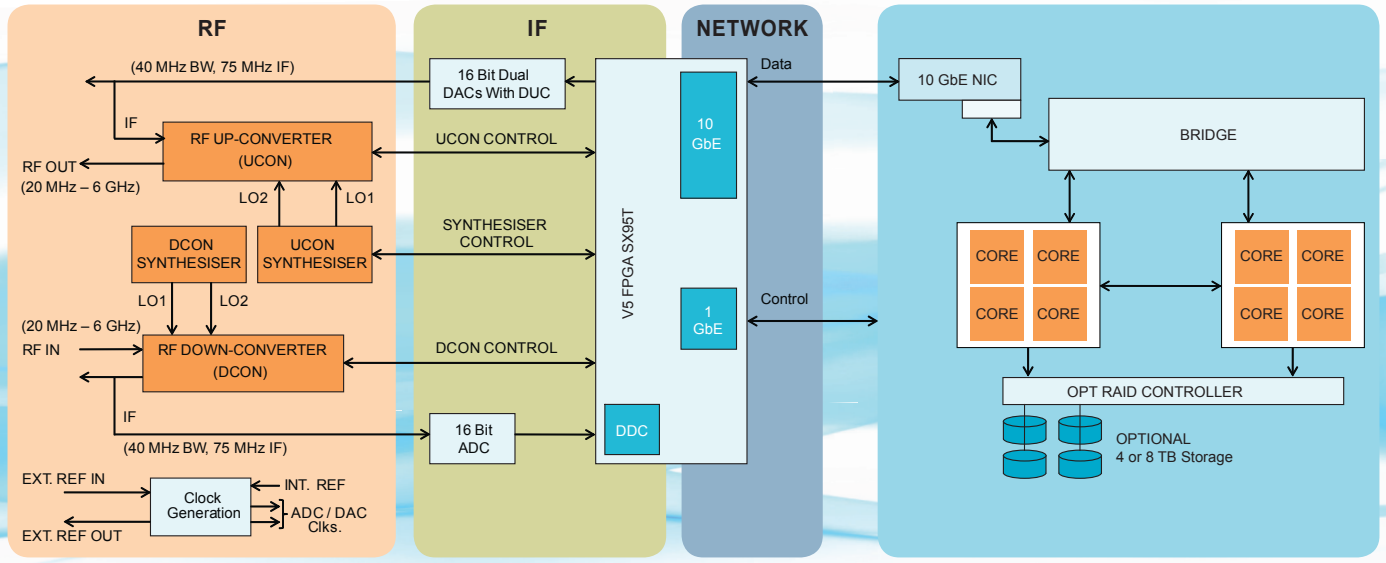

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Phoenix Mission Lander on Mars, artist's concept courtesy of NASA/JPL

Power.org celebrates 20 years of advancing Power Architecture technology

By Staff Editor

In the 20 years since Power.org was founded, it has achieved notable success in driving collaborative innovation, including a nod as 2010's No. 1 worldwide market share leader in 32-bit MPUs and No. 2 worldwide market share leader in 64-bit CPUs. Key to these achievements are Power Architecture's diverse range of next-gen technologies, in addition to its burgeoning road map and ecosystem. The organization believes these factors will ensure market strength in 2011 and beyond.

Power.org, the organization that promotes and develops standards for Power Architecture technology, cited 2010 as a year of continued global growth and adoption for Power Architecture technologies in the automotive, compute, consumer, high-performance computing, industrial, medical, military and aerospace, wired communications, and wireless communications markets.

According to IMS Research's 2010 "The Comprehensive Processors World Report," Power Architecture products represent $4.4 billion of the total 32/64-bit microprocessor market and ranked as No. 1 worldwide market share leader in 32-bit MPUs and No. 2 worldwide market share leader in 64-bit CPUs. Power.org reports that since 1991, more than 1 billion Power Architecture technology-based chips have been built into electronics equipment such as enterprise switching and routing, base station equipment, game consoles, printers and images, network storage, access points, cars, industrial automation, servers, high-performance computers, and more. This represents remarkable growth since Power.org's formation in 2005 and since Power Architecture technology was introduced 20 years ago.

Initially, Power.org focused on merging the three-volume PowerPC Architecture Book – which defined the instructions and registers used by application programs, the storage models, privileged facilities, and related instructions for the IBM POWER5 processor family – into the Power Instruction Set Architecture (ISA) series. This series addresses both the server and embedded spaces for 32-bit and 64-bit architectures. Power ISA 2.03, 2.04, 2.05, and 2.06 were published from 2005 to 2009, to advance and support multicore, virtualization, hypervisor technology, and power management. Power ISA Version 2.06 Revision B, introduced in 2010, allows multiple operating systems to run over multiple embedded cores, providing the requisite isolation and protection while increasing performance through full hardware virtualization. This *full virtualization* (aka *virtual CPU*) does not require any modification in a guest OS.

In addition to the evolution of Power ISA technology, Power.org – with the collaboration of its member companies – has developed a series of technical specifications aimed at lowering costs and speeding software development. These specifications include Power Architecture Platform Requirements for Embedded and Server (ePAPR, sPAPR), Common Debug Interface API specification, and the Physical Connection for High-speed Serial Trace specification aimed at improving efficiency and simplifying the debug process. In 2010, the organization released sPAPR v2.4, which improves the

operation of previous versions and adds new functionality such as the Cooperative Memory Over-commitment (CMO), I/O Super Page, and Virtual Processor Home Node (VPHN) options.

Diverse range of next-gen technology

The collaborative nature of Power.org and the ongoing delivery on a silicon road map by the organization's members have enabled Power Architecture technology to address next-generation, high-performance systems requirements across diverse applications such as networking, game consoles, and some of the most energy-efficient supercomputers in the world. Market highlights include the following:

- **Automotive** – More than 50 percent of all new car models, such as Ford and BMW, contain Power Architecture-based controllers in drive trains, telematics, and safety systems.
- **Compute** – Power Architecture is used in some of the fastest (5 GHz) and most resilient enterprise servers – including the Power Servers 4, 5, 6, and 7. "IBM WebSphere middleware on POWER7 hardware can get the lowest cost for performance in the industry – one-third that of the nearest competitor," according to IBM (see www-03.ibm.com/press/us/en/pressrelease/33964.wss). IBM's "Watson" computing system based on POWER7 was used to challenge all-time greatest "Jeopardy" champions.
- **Consumer** – Power Architecture technology is the core of the newest generation of innovative game consoles (Xbox 360, Wii, and PS3). In 2010, members drove the first Android OS port, which is now available as open source code for the embedded community.
- **High-performance computing** – Two of the top 10 and five of the top 20 of the world's most powerful supercomputers are Power Architecture based (www.top500.org). IBM Blue Gene/Q, the "Greenest Supercomputer in the World," and 13 of 25 power-efficient systems at 1,684 MFLOPS/watt are also Power Architecture based (www.green500.org).
- **Military and aerospace** – Power Architecture technology is the only architecture to be used in every space mission to Mars including the Spirit and Opportunity Mars rovers, the Mars Pathfinder lander, the Mars Polar Lander, the STEREO spacecraft, the IMAGE/Explorer 78 MIDEX spacecraft, and the Phoenix Mars Polar Lander.
- **Wired communications** – The Power Architecture serves as core embedded technology and intelligence for 50 percent of enterprise/core communications networks for switching and routing equipment among companies such as Huawei, NEC, and H3C.
- **Wireless communications** – Power Architecture technology is the *de facto* standard in the embedded telecom-in-wireless infrastructure market, suited to high-performance, low-power SoCs (multicore processing, virtualization, and energy management) with companies such as Alcatel-Lucent and Datang.

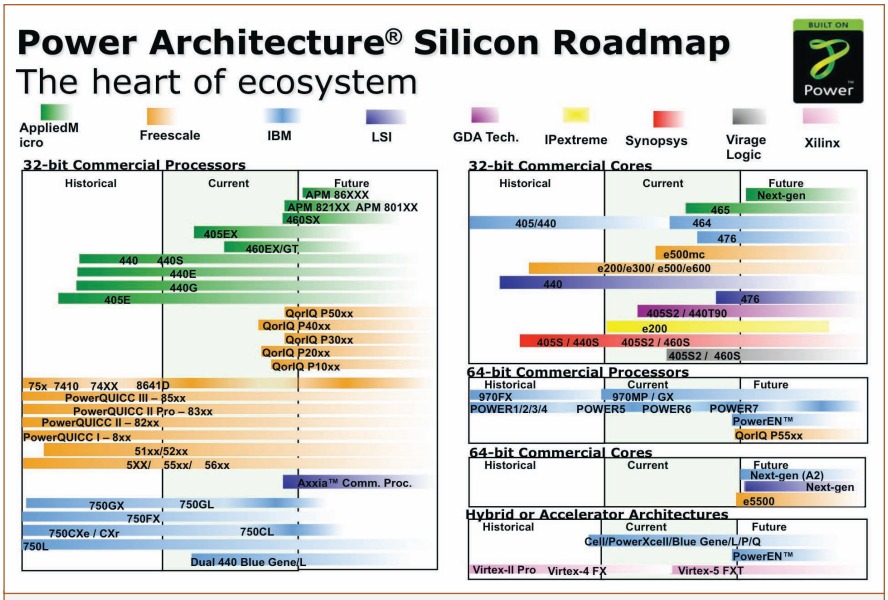


Figure 1 | Power.org members delivered on the Power Architecture silicon road map, with several product announcements and member alliances.

Burgeoning road map, products, and ecosystem

As Power Architecture technology enters its third decade, it will be driven by the Power Architecture silicon road map introduced in 2010. This road map includes major silicon commitments from the members of Power.org including IBM, Freescale, Applied Micro, and LSI Corporation, as well as companies licensing Power Architecture core technologies. The Power Architecture silicon road map extends the architecture's focus on scalability, reliability, and flexibility. In addition, the road map presages performance gains because of an emphasis on multicore and accelerators as well as power management and hardware virtualization, enabling multiple operating systems to operate over multiple cores in both 32-bit and 64-bit architectures.

According to Fawzi Behmann, Director of Marketing and Strategic Advisor for Power.org, "Power Architecture ecosystem members have delivered a clear message: They are committed to ensuring the availability of the products needed to build systems leveraging the Power Architecture standard."

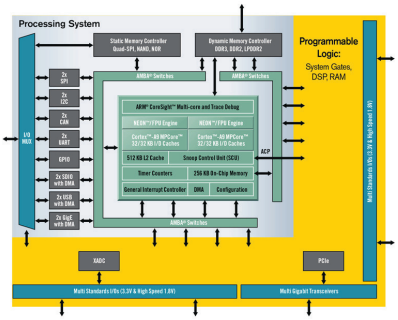
Power.org members delivered on the Power Architecture silicon road map (Figure 1) with product announcements from Applied Micro, IBM, Freescale, and LSI Corporation; alliances among Freescale, Enea, Green Hills Software, and Mentor Graphics; and awards including the U.S. National Medal of Technology and Innovation, bestowed upon on the Power Architecture-based IBM Blue Gene family of supercomputers (www-03.ibm.com/press/us/en/presskit/28422.wss).

2011 and beyond

In 2011, Power.org plans to approve and release the Application Binary Interface (ABI) document, which describes the low-level interface between applications and the system. The Power ABI should include information that is in both the embedded ELF ABI and the Linux ABI. It will be licensed under the GNU. In addition to full virtualization introduced in 2010 through the Power ISA 2.06 Rev. B, the organization's technical committee is planning to introduce a Hypervisor API (h-call interface) as part of the ePAPR specification. This is intended to allow the guest and the hypervisor to communicate in a standardized way.

HOTTEST PRODUCTS

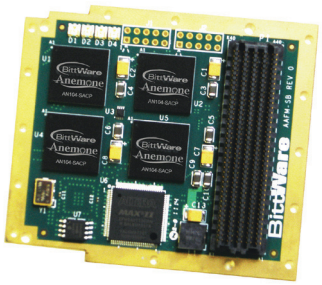
Xilinx tosses in the kitchen Zynq for new ASSP class



With Xilinx's MicroBlaze CPU nearing retirement, the latest 28 nm Kintex-7 device sports dual ARM Cortex-A9 CPUs plus peripherals and I/O. Instantiated as hard logic, the first-ever Zynq-7000 Extensible Processing Platform is a programmable ASSP and comes with 800 MHz CPUs, USB I/O, flash memory, AES and SHA 256-bit encryption, dual 12-bit A/Ds, Gen 2 PCIe, and between 154 and 404 user I/O. There's also 4 to 12 Gigabit transceivers. As for the FPGA portion, size ranges from 28 K to 235 K logic cells (up to 3.5 M equivalent ASIC gates), up to 1.86 MB of Block RAM, and a whopping 912 GMACS of peak DSP performance (in the largest Kintex-7 FPGA).

Xilinx **www.xilinx.com**

Sea of gates: BittWare's Anemone does floating point



The classic coprocessor model still offers performance advantages when it offloads an Altera FPGA. BittWare's Anemone ASSP floating-point coprocessor is based upon Adapteva's Epiphany architecture. The 16-processor ("eCore") ASSP boasts 32 GFLOPS at only 2 W. Designed for processor-intensive, single-precision IEEE 754 FP computations, the shared memory eMesh architecture focuses strictly on computation. With the chip's external high-speed I/O and memory subsystems, 8 TFLOPS are available if 4096 processors are ganged together. Anemone is programmable in C via GNU tools and Eclipse multicore IDE. BittWare intends to use Anemone in a line of FMC (128 GFLOPS @ 10 W), AMC, VPX, and PCIe slot cards.

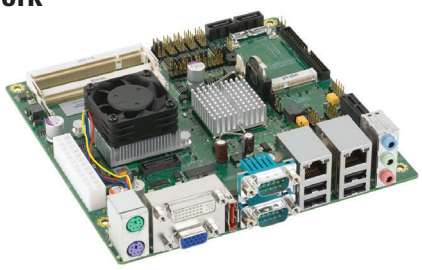
BittWare **www.bittware.com**

INTEGRITY Security Services: New business unit

Green Hills' INTEGRITY and INTEGRITY-178 RTOS offerings are well recognized among the industry's most secure operating systems, even NIAP certified to EAL6+. Now Green Hills is taking their 29-year success story in a new direction: INTEGRITY Security Services (ISS). This business unit follows the company's other security subsidiary, INTEGRITY Global Security, which sells hardened computer and enterprise environments. ISS will sell "end-to-end security solutions for [embedded] devices." Of note are the ISS Toolkits providing FIPS-compliant crypto primitives, along with a complement of security protocols. The tools emphasize: authentication, authorization, network access control, confidentiality, integrity (of course!), and remote management. Existing INTEGRITY customers get the kits free for 12 months.

Green Hills **www.ghs.com**

Avnet's Performance Matched Kits remove guesswork

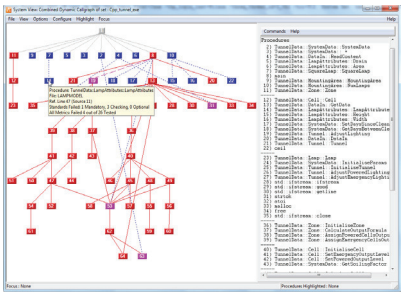


Remember when distributors sold chips and held inventory? Today, the world's largest electronics distributor designs systems, makes boards, and shakes out software. That's all for the benefit of designers, so they don't have to. Avnet Electronics Marketing, a group within Avnet, assures us that their Performance Matched Kits contain motherboard, display, peripheral, and support products from myriad manufacturers (like the Emerson MITX-440 Mini-ITX SBC shown here). The kits even contain cables – just add your own power. There's a single part number for the kit, and interoperability between the pieces has been pre-assured. Add-ons like sensors, LCD drivers, EMI shields, and even backlights are also available.

Avnet Electronics Marketing
www.em.avnet.com/embeddedpmk

HOTTEST PRODUCTS

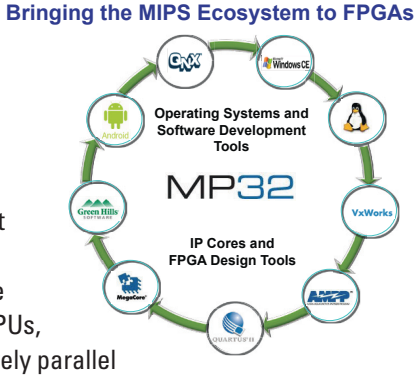
Trace object-to-source for safety-critical code



For systems looking to certify to DO-178C, 510k per the Medical Devices Act, or where legacy code needs to be traced to a requirement, LDRA has an answer. The company claims to offer the first COTS Requirements to Object-Code Traceability tool in existence. Designed for medical, automotive, and avionics systems, the automated tool alleviates the tedious and often hand-created frustration of requirements-to-object-code traceability. While requirements-to-source tools exist (including from LDRA), once a compiler has created assembly (object) code, that tracing link is often hidden. No more. There's now an ability to review code instruction by instruction, which provides transparency, automated documentation, and faster debug times, and can even help map legacy code backwards.

LDRA **www.ldra.com**

Massively parallel CPUs inside Altera FPGA

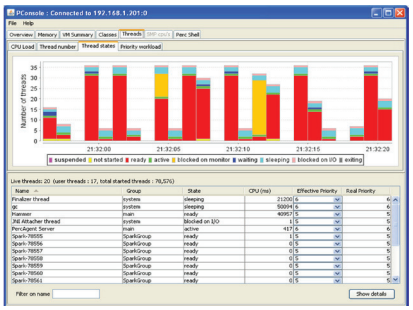


Until Altera's MP32, you couldn't get more than four CPU cores in an FPGA. But using an RTL-based soft MIPS32 CPU, it's possible to realize up to 100 32-bit CPUs, creating a massively parallel device all in an FPGA. Originally aimed at set-top boxes and cellular base stations that crunch lots of DSP algorithms, the MP32 fits radar, sonar, and other C4ISR DoD systems. Available in Aria, Cyclone, and Stratix FPGAs, the device kit is sold exclusively for Altera by partner System Level Solutions (SLS). The development ecosystem is extensive, using Altera, MIPS, SLS, and many other vendors' COTS tools.

Altera **www.altera.com/mp32video**

System Level Solutions **www.slscorp.com**

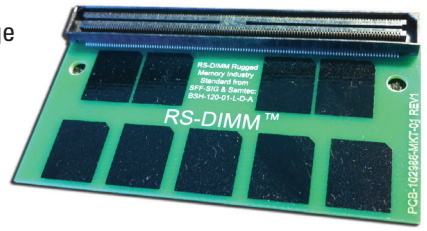
Java shell evolves into real-time console



Atego launched their PERC Ultra 6 Java product at ESC, but what intrigued us the most was the PConsole tool that replaces the un-elegant PShell command line environment. The low-level virtual machine provides point-in-time system characteristics displayed in graphical form for analyzing memory and CPU utilization, number of threads, stack memory, and more. Many metrics can be "drilled down," for instance, providing details about individual threads such as how much of the CPU is being consumed for an individual task. It might not be rocket science, but Java has historically run "mysteriously," so even knowing about the software's garbage collector activity might be hugely useful in an embedded system. PERC Ultra 6 also supports Java 6 and has a new high-speed ahead-of-time compiler plus Virtual File System.

Atego **www.atego.com**

The little (rugged) memory that could

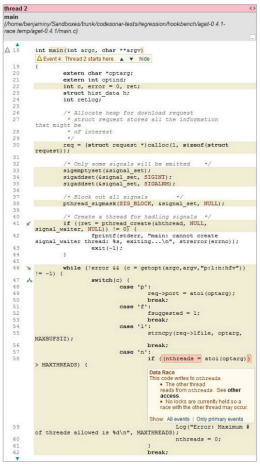


"Stuck on you" – whether a bandage commercial or a song from the '80s – is a poor choice for memory chips if it involves glue or mechanical straps. Yet rugged systems demand robust memory subsystems; COTS systems especially love multiple vendors and interoperability. Enter RS-DIMM, a rugged memory specification from the SFF-SIG and supported by a handful of vendors already. Similar to but smaller than a SO-DIMM module, the 67.5 mm x 7.36 mm module supports DDR3 with ECC, in 9- or 18-chip flavors up to 4 GB. Samtec designed the 240-pin connector, and the whole shootin' match is compliant with ANSI/VITA 47-2005 shock and vibe. A SATA interface is also available for SSDs.

Small Form Factor Special Interest Group (SFF-SIG)
www.sff-sig.org/rsdimm.html

HOTTEST PRODUCTS

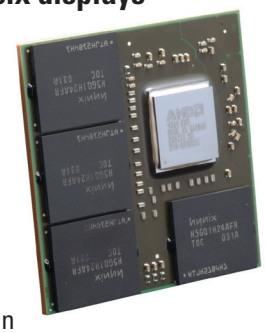
Static analysis now for multicore



Chances are you're already applying static analysis to your code – either for language compliance or to identify questionable code. But now the big deal is multicore concurrent processing, which complicates the process a wee bit with nasty habits like race conditions. GrammaTech has upped the ante with multicore and multithreaded support in CodeSonar, partly funded by a $749,000 DARPA grant. Deep concurrency analysis creates a whole-program interprocedural analysis that captures syntax, call graphs, and control flow. A program model is then created and symbolically executed. The company claims that data race, concurrency defects, and other multicore "tricky bugs" stand a better chance of being identified and hence re-coded.

GrammaTech **www.grammatech.com**

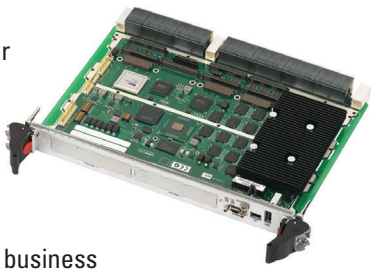
Radeon GPU showcases six displays and OpenCL



Ever wondered how nice it would be to have a wall of LCDs like you see in SitRep Command Centers? It would be great just to have two, but what about six? AMD's Radeon E6760 embedded discrete graphics processor can handle this, along with executing Apple's OpenCL for parallel processing. The 5-year GPU sports 3D graphics and Microsoft DirectX, along with the industry standard OpenCL. The latter helps with portability for radar, sonar, and video surveillance application migration from other CPUs. AMD's Eyefinity technology does the one-to-six display magic, with super-high resolution on each, HDMI 1.4 stereoscopic video, and DisplayPort 1.2 for the highest link speeds. The E6760 works with the AMD Fusion APUs or the company's Turion and Athlon CPUs. We saw demos at ESC and were totally blow away by the capabilities and performance.

AMD **www.amd.com**

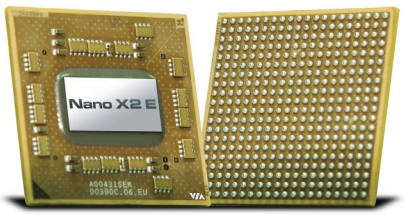
They're back! Dual- and quad-core Core i7 OpenVPX SBCs



Emerson Network Power is the home of VME's spiritual creator, Motorola Computer Group. And now Emerson's thoroughly back in the rugged VME business with this duo of dual- and quad-core Core i7 OpenVPX (VITA 65) SBCs. The iVPX7220 (quad) and iVPX7223 (dual) boards use Intel's Core i7 2655LE CPU with integrated graphics. Available in air- and conduction-cooled versions and from -40 °C to +71 °C or +85 °C, these are loaded boards. In maximum configuration, there's 16 GB of DDR3, GbE to the control plane, and PCIe to the data and expansion planes. There's also 4 GB of USB flash and an unusual 256 KB of Ferro-electric RAM (F-RAM). Up to 9 USB, 5 serial, 5 SATA, 10 GPIO, 3 DisplayPort, VGA, and dual XMC round out the "all dressed" list. Payload profile is MOD6-PAY-4F1Q2U2T-12.2.1-3 and -4.

Emerson Network Power
www.emersonnetworkpower.com/embeddedcomputing

Dual core, 64-bit x86 CPU sports AES



In the x86 market, one has three choices: AMD, Intel, and VIA. The reason for choosing a VIA CPU for embedded comes down to features and power. The VIA Nano X2 E-Series is the company's latest dual-core CPU, and it comes with some features not found in the competition. The native 64-bit superscalar cores (two of them) are efficient at natively running Windows 7 Embedded and can handle large data sets for deeply embedded systems. There's also an efficient speculative floating-point algorithm for number crunching, and a hardware-based AES encryption engine for on-the-fly crypto. Speeds are 1.2 GHz (13 W) and 1.6 GHz (27.5 W), while hardware virtualization (VT) brings legacy code and applications forward with minimal fuss. VIA also supports the X2 E-Series for seven years, and it's pin-compatible with previous generation VIA CPUs.

VIA Technologies **www.via.com.tw**

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OpenVPX: From Specs to Solutions

Presented by: GE Intelligent Platforms, Pentek, Curtiss-Wright Controls Embedded Computing, Curtiss-Wright Controls Electronic Systems

The OpenVPX initiative was started in 2009 in response to a US Department of Defense mandate for improved implementation of open standards and interoperability over the VITA 46 specifications. OpenVPX leverages the existing VPX specifications while further defining areas where existing specifications allow multiple or open implementations that cause compatibility issues during system integration.

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Discover Wind River Linux Secure, the first EAL4+ certified embedded Linux platform

Presented by: Wind River

In this webinar, we're pleased to introduce you to Wind River Linux Secure, the first commercial Linux to achieve Common Criteria EAL4+ certification on three popular embedded hardware architectures: Intel, ARM, PowerPC.

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Modern Practices for Effective Development of DO-178B/C Compliant Software

Presented by: MKS

In this presentation, MKS will provide an overview of the processes and objectives called out by DO-178B. Colin Doyle will discuss practical approaches to addressing these criteria with particular emphasis on the need for traceability, independence criteria, and the use of tools to streamline and automate processes where appropriate.

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Leveraging DO-178C and Reusable Software for Modern Avionics Development

Presented by: DDC-I, HighRely

DO-178C will soon be mandatory for avionics development, and changes will be required throughout the industry. Among these changes, DO-178C has provisions for accepting modern software engineering practices, which enhance software reusability and reduce certification cost and risk.

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DNA
protects electrical components against counterfeiting

By James A. Hayward, Ph.D., Sc.D.

DNA is a form of forensic evidence trusted by law enforcement and recognized by international courts around the world. The following discussion provides an introduction to the utility of botanical DNA taggants to safeguard electronic components in supply chains and to protect against counterfeiting and diversion. A detailed treatment of the science behind botanical DNA technology, along with its application to semiconductors and microchips, is presented.

The evolution of counterfeiting as a trade nearly parallels the evolution of technology itself. The past two decades have witnessed explosive growth of technology, and the condensation of travel, communication, and the massive impact of the Internet ensured these new technologies were laterally propagated instantly across the planet. Now counterfeits emerge on the market nearly simultaneously with new product launches, in time for the counterfeits to benefit from the marketing efforts expended by the original. The World Customs Organization estimated that annual global trade in illegitimate goods was roughly $600 billion in 2004, and was expected to double by 2014, representing between 5 to 7 percent of all world trade (Source: The International Anti-Counterfeiting Coalition). But this is more than a vexing nuisance for brand owners. Counterfeits threaten economies, destroy health and take lives, and destabilize the military.

The *Defense Standardization Program Journal* (Oct/Dec 2009) recognizes the definition of a counterfeit electronic part as "one whose identity or pedigree has been deliberately altered, misrepresented or offered as an authorized product."

In June of 2007, the U.S. Department of the Navy suspected that an increasing number of counterfeit electronics was infiltrating the Department of Defense (DoD) supply chain. In collaboration with the Department of Commerce (DOC), a study was initiated to assess the defense industrial supply base and to determine the statistical frequency of counterfeit electronics penetrating DoD. The results of this study, finalized in January 2010 (U.S. DOC "Defense Industrial Base Assessment: Counterfeit Electronics") showed:

- All elements of the military supply chain have been directly impacted by counterfeit electronics
- Stricter testing protocols and quality practices are required
- The use of authentication technologies by parts manufacturers, distributors, and integrators should be expanded

Current authentication methods are inadequate

Efforts to secure the authenticity of electronics are first encountered at the primary and secondary packaging. Traditional security platforms to prevent counterfeits are now also part of the counterfeiter's target and consequently within the arsenal of counterfeiters' resources. New advances in holograms, optical strips, and RFID are often available as near-perfect copies within days of their initial launch.

Additionally, most distributors and integrators store microchips and semiconductors in high-volume bins. This "bin approach" excludes the packaging to save space and time, so security must be implemented at the product level. Product inspections offer limited value as a method of authentication. Physico-chemical characterizations are often destructive and rely on a degree of similarity to a bona fide original and the tolerance of the measurements.

Taggants can provide a unique code or fingerprint to authenticate originality. However, as evidentiary tools, the value of a taggant increases as a function of the density of its information content.

Mineral taggants, which simply provide parameters of chemical identity and concentration, are only effective as rapid-screening tools, often by handheld detectors. Stochastic arrays of fibers or particles are difficult to incorporate in the media used to fabricate microchips and semiconductors. Stochastic arrays of nanoparticulate ferrite can generate complex "fingerprint" patterns, but care must be exercised to ensure the magnetic field does not interfere with semiconductor function. However, forensic DNA taggants have proven most effective.

"Stochastic arrays of nanoparticulate ferrite can generate complex "fingerprint" patterns, but care must be exercised to ensure the magnetic field does not interfere with semiconductor function. However, forensic DNA taggants have proven most effective."

Forensic DNA as a taggant ensures authenticity

Evolved over eons, Deoxyribonucleic Acid (DNA) provides the blueprint for all of biology. The information content is massive, highly customized by organism, and capable of compaction into infinitesimal space.

Used by forensic laboratories all around the world, including the FBI, DNA authentication is absolute in character. When used to identify individuals or to establish paternity, the error frequency for false positives is less than one in a trillion.

SigNature DNA (forensic DNA) markers cannot be copied or reverse engineered and have already been independently validated through a two-year vetted process conducted by the DoE and the Idaho National Laboratory.

Some mechanisms for protecting DNA in harsh chemical and physical environments are shown in Table 1 – relative to the insertion of DNA into plastics, films, adhesives, inks, and metal surfaces.

Key attributes of SigNature DNA

Applied DNA Sciences has proved that botanical DNA technology provides the following advantages over existing competitive security options:

DNA Markers' Stability Applied DNA Sciences, Inc.		
Test	Test Specifics	Results
UV Energy	Equivalent to more than 350 years of UV energy accumulation in Denver	Stable
X-ray	4 times the X-ray exposure by scanning machine in an airport	Stable
y-ray	30 kGy (kilo-Gray) radiation exposure by y-ray sterilization machine	Stable
pH Thermal	Exposed to pH of 1 to 14 overnight	Stable
Thermal	Up to 250 degrees Celsius	Stable

Table 1 | Some mechanisms for protecting DNA in harsh chemical and physical environments, relative to the insertion of DNA into plastics, films, adhesives, inks, and metal surfaces.

- **Resistant to reverse engineering or replication.** The botanical SigNature DNA platform is virtually impossible to copy. The DNA segment used in the taggants needs to be replicated billions of times for detection and identification to take place, a process that can only be achieved by applying matching strands of DNA.
- **Low cost and high accuracy.** SigNature DNA taggants are relatively inexpensive when compared to other anti-counterfeiting devices, such as RFID, integrated circuit chips, and holograms. The costs associated with the production of DNA taggants are not significant since the amount of DNA required for each taggant is small, and the cloning of the DNA segments is performed inside microorganisms such as yeast or bacteria, which are highly productive and inexpensive to grow.
- **Easily integrated with other anti-counterfeit technologies.** SigNature DNA taggants can be embedded into RFID devices, labels, serial numbers, holograms, and other marking systems using inks, threads, and other media.

Industry deployment of DNA markers

As shown in Figure 1, the procurement entity within the electronics industry typically services a range of end users and would engage Applied DNA Sciences in the DNA marking process. Applied DNA Sciences would work with trusted supply chain participants, including, but not limited to, the integrator, distributor, and Original Component Manufacturers (OCMs) and create unique DNA markers to be embedded into the microchip. Statistical confidence levels are established to determine authentication parameters. Lab analysis is then performed, typically in a non-destructive manner, at any point along the logistics chain. The analysis would absolutely distinguish between genuine and counterfeit components and unequivocal forensic ID would be declared. The result would be authentic components in the end users' product with counterfeit components segregated and supported with forensic proof should legal action be deemed appropriate.

Dr. James A. Hayward *is Chairman, President, and CEO of Applied DNA Sciences. With more than 20 years of experience in the biotechnology, pharmaceutical, life science, and consumer product industries, he works to ensure the authenticity of products and protect global supply chains from counterfeiting. He received a Bachelor's degree in Biology and Chemistry from the State University of New York at Oneonta, his Ph.D. in Molecular Biology from the State University of New York at Stony Brook, and an honorary Doctor of Science from the same institution.*

Applied DNA Science
631-444-6293
www.adnas.com

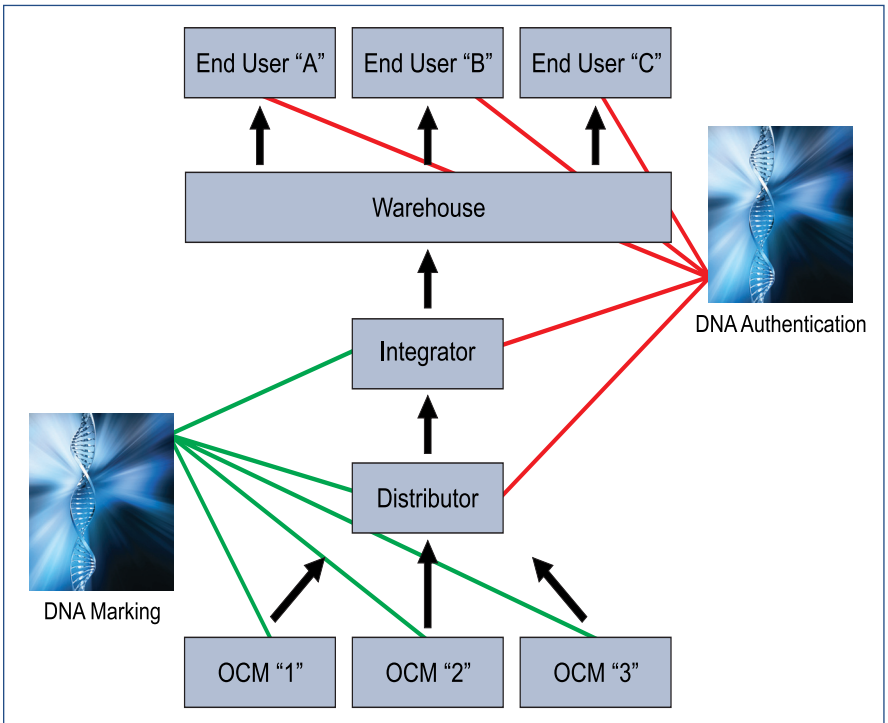

Figure 1 | The procurement entity within the electronics industry typically services a range of end users and would engage Applied DNA Sciences in the DNA marking process.

For more information on the two military imperatives of security and anti-counterfeiting, check out these articles in *Military Embedded Systems* magazine:

Silicon uniqueness as a security feature
By J Ryan Kenny, CPU Tech
www.mil-embedded.com/articles/id/?5167

Strategies for mitigating the threat of counterfeit devices
By Steve Edwards, Contributor
www.mil-embedded.com/articles/id/?4972

U.S. Marines photo by Sgt. Deanne Hurla

Editor's note: Our MES Mar/Apr edition was chock-full of laser-focused UAV articles and interviews, constituting Part 1 of our special coverage on "Controlling the UAV overhead." As promised, here we present Part 2 of 2, comprising articles from Kontron and Mercury Computer Systems.

Deploying ruggedized platforms for unmanned vehicles

By David O'Mara

COTS-based technologies and associated thermal management wares are helping to arm modern UAVs/UASs with built-in harsh environment survivability and reliability, in addition to facilitating effective implementation of video and storage needs.

The evolution of Unmanned Aerial Vehicles and Systems (UAVs/UASs) for Intelligence, Surveillance, and Reconnaissance (ISR) has proven a fundamental game changer for the military. Capable of remote operation, these unmanned vehicles also present some of the most difficult design challenges. This is because of the need to package a high level of computing power and data collection/distribution elements within minimal Size, Weight, and Power (SWaP) constraints, while maintaining ruggedized capabilities to operate in very demanding environments.

Furthermore, the capabilities of UAVs have moved dramatically beyond their original "drones" purpose to now feature advanced onboard intelligence, capable of highly autonomous flight with the ability to make real-time mission adjustments. The complexities of these new UAV/UAS-based systems necessitate high-performance, high-bandwidth computing technologies that just add effective thermal management to the list of design challenges.

According to the unclassified USAF Flight Plan 2009-2047, "standards and interoperability are keys to the Joint Forces gaining informational superiority in today's network-enabled environment." As a result, UAV development goals mandate a common set of airframes based on standard interfaces and interoperable "plug and play" payloads. This mandate for interoperability calls for an open architecture COTS approach. However, the range of airframes deployed along with their accompanying ground command and control systems demands that designers develop a deep understanding of application- and system-level options.

New embedded computing COTS-based technologies and their associated thermal management solutions are helping to advance UAV/UAS design. Two considerations are paramount: building in harsh environment survivability and reliability and designing for video and storage needs. COTS-based options can help overcome developmental challenges to achieve tightly integrated systems that match the military's unified network-enabled objectives and its ISR mission goals.

Technology drives enhanced UAV/UAS capabilities

One of the first important considerations in UAS/UAV development is evaluating the broad range of new platforms and system-level technologies that provides increased computing and communications capabilities and greater real-time operational control. UASs include ground stations and other elements besides the actual UAV aircraft, so embedded platforms must be able to support multiple tasks, as opposed to military designers having to develop multiple systems dedicated to separate tasks. As an example, UAS reconnaissance programs must include multiple functions such as vision systems, heat sensors, electromagnetic spectrum sensors, biological sensors, and chemical sensors.

Feature-packed, high-performance and high-bandwidth embedded computing solutions combined with high-density storage capacity can handle the computationally intensive demands of massive and ever-increasing amounts of sensor data. Military system designers are continually turning to proven, standards-based platforms such as Computer-on-Modules (COMs), CompactPCI, and VPX to reach their ISR interoperability program objectives. However, each must also be weighed for its ability to meet SWaP and thermal management requirements of the airframe and its mission.

For instance, smaller airframes with high performance requirements are ideal candidates for COMs-based solutions. There is a range of new Intel Core i7 processing-based COMs that offers increased processor efficiencies and delivers better signal integrity and increased performance for these space-constrained UAV designs. Providing a significant breakthrough for compute- and graphics-intensive imaging or surveillance UAV/UAS applications, these new COMs have improved data flow performance due to a new integrated chipset and advanced display interfaces.

Key UAV application requirements

Each defined airframe has specific requirements that will vary with its unique operational objectives; however, there are certain key requirements that are critical to successful deployment of embedded computing systems for ISR programs.

Harsh environment survivability and reliability

The benefits of new sophisticated features in UAVs in ISR applications will be elimi-

nated if the system is not able to operate continuously and reliably within its target environment. The design approach that has proven most effective over time is to place the embedded computing technology in a chassis or enclosure manufactured to MIL-901D shock and MIL-167-1 vibration. That way, it can withstand specified vibration, shock, salt spray, sand, and chemical exposure in harsh environments.

Another rugged consideration is that a standardized COTS chassis can be adapted to meet specific cooling needs in mobile applications. Because of SWaP and environmental constraints, many UAV designers opt for conduction-cooling methodologies (with or without fan assist), but other methodologies are available. Accordingly, Table 1 gives a general set of guidelines indicating how many watts per inch of pitch are dissipated with each cooling method. But because each application has its own unique thermal equation, an important consideration is the ability to leverage pre-qualified MIL-E-5400 COTS platforms that can also be customized and tailored to fit specific airframe or program requirements.

The choice of cooling method is primarily driven by the total power dissipation; however, in airborne applications, ambient pressure is important because air density plays a major role in system thermal efficiencies of forced-air or passive convection-cooled enclosures. Liquid cooling is used only for situations that either operate at very high power levels or have no air or cold plates available. However, the increased system cost and lower overall MTBF of liquid-cooled systems are important considerations and need to be analyzed against simpler solutions.

Designing for video and storage needs

The sheer amount of visual content and other data routinely collected by UAVs would have been unthinkable just a few years ago. Plus, the demand for real-time remote monitoring as well as the integration of attack capabilities require a much higher level of computational performance. Besides collecting and storing data, onboard systems must be able to stream visual information in real time. Thus, the computational performance needed to support these massive data rates must be exceptional.

For these real-time imaging applications, VPX offers higher bandwidth processing using serial switched fabrics that enable significant improvements to subsystem application performance. VPX-based

Power dissipation by cooling method	
Thermal management option	**Performance (watts per inch of pitch)***
Conduction cooled – Passive convection (no fan)	25
Conduction cooling – Cold plate	50
Conduction cooled – Air blown through chassis side walls (fan or plenum)	75
Convection cooling – Air blown (fan or plenum air)	100
Conduction cooled – Liquid cooled through chassis side walls	125
Conduction cooled – Liquid flow through modules	500
Spray cooling – direct impingement on ICs	700

*depending on ambient conditions

Table 1 I General guidelines for the approximate power dissipation of various cooling methodologies. Ambient temperature, altitude, generated power, and other environmental factors can create notable variations to these approximate values.

platforms offer higher-performance processing per slot and higher-speed interconnects between processing and I/O elements using PCI Express, 10 GbE, or Serial RapidIO. These interconnects provide 10 Gbps between elements or several hundred GBps in aggregate, depending on the system implementation. VPX also can be integrated with codecs such as ITU-T H.263, H.264 (MPEG-4 part 10), and JPEG2000 to provide very efficient image compression. Considering the variety and availability of COTS products, some applications might best be designed using more than one bus structure. For example, a CompactPCI switch can be used with a VPX-based board by utilizing a hybrid backplane.

Modular, high-density SSD-based storage subsystems are also being deployed to effectively handle large amounts of data and support quick-swap exchanges for rapid mission debriefing and/or mission turnaround – versus waiting to download the data through the I/O connection. It is important to note, however, that specific airframe configuration requirements might arise and necessitate a custom backplane design with I/O routing options. For example, the positioning within the system is critical for heat-generating VPX boards and power supplies to effectively manage the heat loading requirements, and might require a customized cooling solution or demand the chassis is cooled and mounted in a specific manner.

Figure 1 | Designers can configure the COBALT for either 28 VDC or 115 VAC input power for compatibility with a broad range of UAV/UAS ISR applications.

Finding the optimal COTS solution

Whether a designer integrates a COTS-based platform or uses one as the basis for a custom UAV/UAS design, both offer future scalability. More importantly, COTS technology advancements provided by COMs, CompactPCI, and VPX-based COTS platforms and the evolution of viable cooling methods and enclosures ensure that the expanded ruggedization, network-enabled, real-time imaging expectations for today's UAV/UAS designs are ready to be deployed in ISR programs. An example of a COTS-leveraged platform suitable for UAS/UAV development is the module-based Kontron COBALT (Figure 1), which allows designers to scale computing performance from a 5 W Intel Atom processor-based COMs implementation to an Intel Core 2 Duo system at 25 W.

Reusing proven technology enables faster development and higher reliability, and facilitates greater design flexibility while continually feeding future design innovation.

David O'Mara *is Product Manager, Conduction Cooled Products at Kontron. He has a diverse engineering background that includes extensive experience with military and aerospace electronics packaging, pressure and accelerometer sensor design, and high-pressure solid-state physics. David earned his Bachelor of Science degree in Physics from UCLA. Contact him at David.omara@us.kontron.com.*

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New demands on ISR require new technologies and systems

By Brian E. Perry

U.S. Air Force photo by Lawrence Crespo

Defense prime contractors building highly advanced systems for the DoD are facing the perfect storm of challenges: enemy threats that require highly sophisticated and advanced technology in ISR systems coupled with Defense Acquisition Reform (DAR) guidelines that demand shared risk and the delivery of better solutions, faster and for less money. To weather this storm requires an entirely new, open standards based, approach.

Military strategists consider this the most dangerous time in history for warfighters, not so much because it is known precisely which threats exist, but because the types of threats faced are exponentially more challenging to anticipate and diffuse than in any previous period. Today, tracking smaller, faster targets requires ISR systems to provide exact and minute imaging details to help forces find and fix an elusive enemy. In fact, the DoD is demanding more ISR "assets" as a means to find, fix, and finish unconventional enemies. At the same time, Defense Acquisition Reform (DAR) directives from the DoD are requiring Fixed Price Incentive Firm (FPIF), shortened development cycles, open standards technologies that are easily upgraded over time, and upgrades to existing platforms over building new ones. According to the famous quote by Dr. Ashton Carter, Under Secretary of Defense for Acquisition, Technology, & Logistics, DAR comprises the need for the military to "do more without more."[1] Under DAR guidelines, prime contractors will have to share more risk by working with FPIF contracts, and smaller businesses will have the opportunity to play a larger role in DoD opportunities.

Changing threats and DoD demands have spawned a new class of technical challenges in the development of ISR systems and driven new open standards approaches, as the presented case study illustrates.

ISR technical challenges escalate

Bringing actionable ISR information to the tactical edge requires the ability to collect accurate data from multiple persistent perspectives, fuse it into meaningful facts, and identify an elusive enemy. Sophisticated sensors have the ability to survey increasingly wider areas and deliver data and images with incredible detail, providing tremendous volumes of multisensor data that can delay existing tasking, processing, exploitation, and dissemination systems.

The sheer amount of data would require thousands of analysts deployed across the globe to analyze and interpret it, and it would never meet the critical need for virtually instantaneous actionable intelligence to find, fix, and finish imminent threats. Coupled with that is the move toward Multi-Intelligence (MULTI-INT), combining data input from multiple sensors and platforms in real-time to improve situational awareness and reduce time to actionable information. The challenge is to create integrated systems that can extract truly critical information through real-time signal processing and deliver it to warfighters.

Under the current Concept of Operations (CONOP), surveillance platforms have downlink capabilities or the ability to transmit signals from a satellite or airborne platform to a ground station. However, these capabilities are extremely limited in terms of bandwidth. In addition, the human capacity to analyze the information in a timely manner is also limited. Typically, if 100 TB of sensor data is collected during a mission, only about 100 GB of that data is analyzed (approximately 0.09 percent). An emerging, more efficient way is to integrate advanced processing on the platform and perform the initial stages of processing and exploitation directly onboard,

rather than on the ground. Then, critical intelligence is disseminated as needed. Using the more efficient second method, the platform sorts and analyzes the data, tags information for closer review, possibly compresses the information depending on bandwidth and channel requirements, and transmits it immediately to analysts on the ground and to forward-deployed personnel.

Figure 1 shows an example of such an implementation. There are many possible routes that the Electro-Optical/Infra-Red (EO/IR) data can travel to reach its destination. Onboard exploitation is performed on the EO/IR sensor data; this exploited information can be used by the analyst if delays that are incurred by the channel are acceptable. Compressed and exploited data can also be sent to the analysts and forward-deployed personnel to improve situational awareness. Finally, both raw and exploited data can be compressed and stored, and optionally sent to analysts and forward-deployed personnel as forensic data.

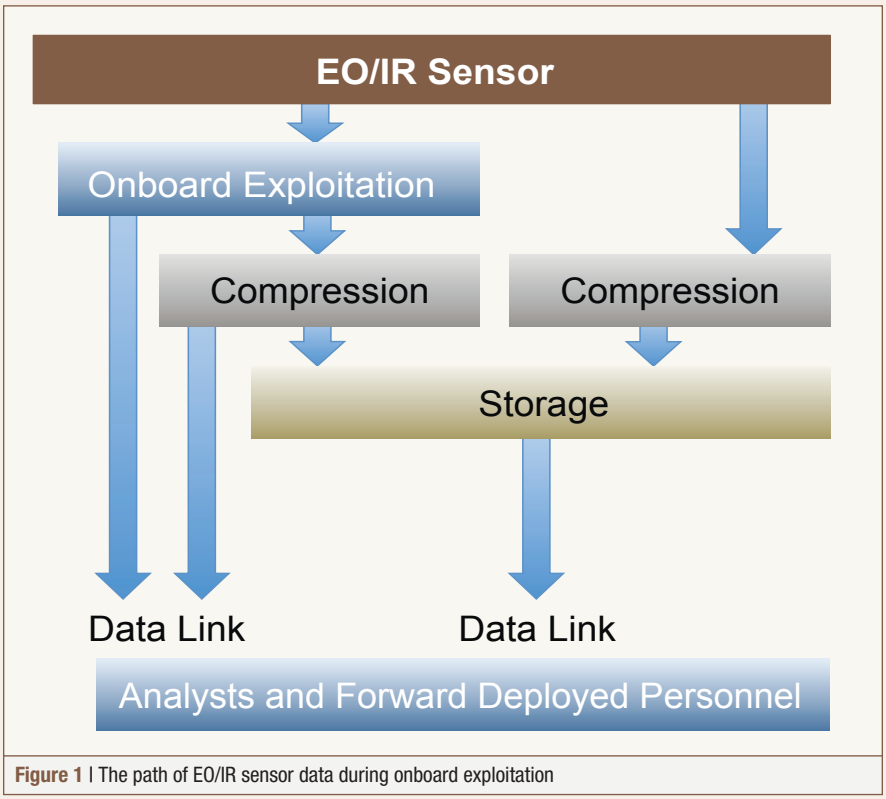


Figure 1 | The path of EO/IR sensor data during onboard exploitation

In addition to specific technical challenges like these, DAR is demanding more innovative solutions and requiring open systems, which reduce cost, increase interoperability, simplify upgrades, and allow vendors to choose components based on cost/performance instead of being locked into a proprietary architecture.

Case study: One year to flight test

Recently, a prime contractor won a highly time-sensitive Quick Reaction Capability (QRC) DoD contract, which required the delivery of a prototype imaging subsystem capable of supporting flight test within one year of receipt of the contract. The highly Size, Weight, and Power (SWaP) constrained subsystem would ultimately be installed aboard a Medium Altitude Long Endurance (MALE) UAV and required multiple advanced electro-optical/infrared sensors.

To meet these constraints, much of the multi-image processing and exploitation capabilities had to reside onboard the platform (onboard exploitation). The real-time and computationally intensive algorithms that comprised onboard exploitation were intended to derive actionable information from streaming sensor data, reducing analyst processing time, mitigating bandwidth and storage requirements, and delivering situational awareness to the warfighter. The application called for greater onboard compute density (in terms of GFLOPS per watt) than existing technologies could deliver; for example, typical CPU architectures deliver less than one peak theoretical GFLOPS per watt – much less than is required for such an intense multi-image application. Additionally, data storage units for image compression and forensic data storage were needed.

"The application called for greater onboard compute density (in terms of GFLOPS per watt) than existing technologies could deliver; for example, typical CPU architectures deliver less than one peak theoretical GFLOPS per watt – much less than is required for such an intense multi-image application."

The implementation of the required onboard exploitation tasks was a unique challenge. It was decided that transferring the image-processing tasks from a hardware implementation to an algorithmic-based implementation would deliver a faster, more reusable and upgradeable solution. Product line building blocks from Mercury, including GPU processor boards, single board computers, and switch boards, formed the initial backbone of the subsystem.

To secure the required compression and camera interface technology, best-of-breed open standards XMC components were chosen from third parties. Mercury then designed, developed, and tested a 96 TB data storage unit. This open standards approach mitigated the life-cycle costs of a proprietary approach. The result was a

Figure 2 | A high-performance Application Ready Subsystem (ARS) that interfaces with complex sensors and data storage

high-performance, conduction-cooled, 6U OpenVPX Application Ready Subsystem (ARS) that interfaces with complex sensors and data storage (Figure 2). An ARS is an open standards, application ready, MULTI-INT subsystem for the ISR market. These subsystems comprise building blocks that optimize performance and meet SWaP constraints. Every ARS is derived from hardware, software, services, and systems integration and is designed for a specific application area such as EW, radar, EO/IR, or C4I.

Essential technology for ISR/DAR

An ARS provides very high technology and manufacturing readiness levels, reduces costs, and shortens development cycles. And because it is based on open standards, it is easily upgraded over time. These are all critical considerations in budget-sensitive, FPIF environments, where the DoD is demanding shorter program implementation times for ISR systems, favoring upgrading existing platforms over building new ones, and forcing prime contractors to focus on a project's entire life cycle.

Reference:

[1] "Better Buying Power: Guidance for Obtaining Greater Efficiency and Productivity in Defense Spending," Sep. 4, 2010, http://www.acq.osd.mil/dpap/cpf/docs/USD_ATL_Guidance_Memo_September_14_2010_FINAL.PDF

Brian E. Perry *is Director of Services and Systems Integration at Mercury Computer Systems. In this role, he is responsible for all aspects of the services-led, system-level engineering and manufacturing operations. Prior to joining Mercury, Brian was the General Manager for Suntron Corporation's Northeast Express, which included responsibility for advanced prototyping, design services, and systems engineering and integration. Perry holds a Bachelor's degree in Aeronautical Engineering from Worcester Polytechnic Institute and an MBA in Management of Technology from Bentley College.*

Editor's Choice Products

Editor's note: Military Embedded Systems *is "hip" to the whole Web 2.0 social networking revolution. While we don't know which of today's buzzy trends will last, we're going to start including links to vendors' social networks, when provided. You can also reach us on Twitter, Facebook, and LinkedIn ... and that's just for this week. Next week there'll undoubtedly be more new sites.*

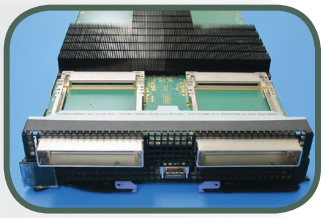
Operation Enduring Freedom wearable computer now COTS

It's a hassle for soldiers to have to switch gears (literally), going from operating a computer one minute to suiting up to engage in combat the next. Such packing and repacking batteries and computers takes time and adds weight to the soldier's ensemble, and Black Diamond Advanced Technology's wearable, MIL-STD-810-G and MIL-STD-461F compliant Modular Tactical System (MTS) stops these slowdowns. Operationally proven in Operation Enduring Freedom by Special Ops groups, MTS is vended presently as a COTS ware (or is that "wear"?).

Specifically, the MTS vest configuration starts with a Tactical Mission Controller (TMC) comprising these notables: a power manager, an Intel Atom 1.6 GHz-based processing platform with 2 GB RAM and 128 GB removable SSD, and a peripheral controller. Software includes an intuitive interface that presents C2/SA info adeptly on a single display. TMC rides on back of the plate carrier, and an interchangeable cummerbund houses the computer cables and also mounts onto a plate carrier. A tactical hub for rangefinder and other mission peripheral interfacing is additionally cummerbund routed. Meanwhile, a 6.5" Night Vision Goggle (NVG)-compatible, sunlight-readable Universal Tactical Display (UTD) is housed in a flip-down front pocket. And those batteries already carried by the soldier power-up the system, eliminating any need for redundant batteries. MTS weighs a mere 1.8 to 3.5 lbs, and vehicle and bag configurations are also available.

Black Diamond Advanced Technology • www.mil-embedded.com/p52372 • www.bdatech.com

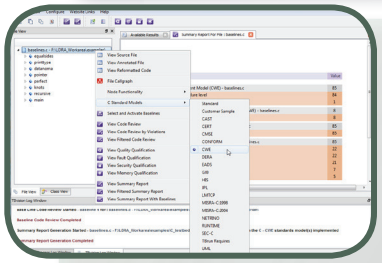
"I'll take data capture and processing for 240 Gbps, Alex ..."



OK it's not really the Alex Trebek-hosted TV game show "Jeopardy"; it's real warfighter jeopardy, and the Signals Intelligence (SIGINT) processing arena is paramount in capturing and processing vast volumes of mission-critical data. Accordingly, stepping into the fore is Annapolis Micro Systems, Inc.'s multi-stream capable Dual 40/100Gbit CFP Transceiver Board, rendering real-time data processing, buffering, capture, and/or transmission facilitated in two ways: either six 40 GbE streams on a card or via a duo of 100 GbE streams on a card. Annapolis credits the either one- or two-Altera Stratix IV GT EP4S100G5 FPGA configuration as a key factor in the board's ability to satisfy the need for speed. Combine those FPGAs with up to 36 GB of DDR3 DRAM in an up-to-eight 72-bit port array and fold in a 160 x 160 high-speed crossbar and watch this transceiver board roar.

And that's not all. The transceiver board's cage interfaces are compatible with the 100Gbit UTU4, QDR InfiniBand, and SDH/OTU3 protocols, and the board's 68 high-bandwidth full duplex serial I/O connections (at 11.3 Gbps) facilitate mating to Annapolis' WILDSTAR 5 Blade for IBM BladeCenter. This serial I/O connectivity enables a received-data bandwidth up to a blazing 240 Gbps, and said data can then be transmitted and processed by up to eight Tilera Network Processors or FPGAs housed on WILDSTAR 5 Blade for IBM BladeCenter. The important thing here is that data reduction and data filtering are no longer needed with this transceiver board.

Annapolis Micro Systems • www.mil-embedded.com/p52167 • www.annapmicro.com



Software tool suite achieves Homeland Security compatibility

In this age of Internet-connected everything, software becomes increasingly vulnerable to security breaches. However, the U.S. Department of Homeland Security's National Cyber Security Division and the nonprofit MITRE Corporation have created and manage the Common Weakness Enumeration (CWE) Compatibility achievement just earned by LDRA for LDRA's tool suite. CWE is an international-in-scope strategic initiative to identify and formally list core software weaknesses that lead to software security vulnerabilities. CWE also aims to create and foster automated tools capable of preventing, fixing, and identifying such software flaws; thus, LDRA's tool suite – including its dynamic and static analysis tools, along with its TBvision and LDRA Testbed – falls into lockstep with this goal.

To achieve CWE compatibility, LDRA had to synch up the LDRA tool suite with CWE coding rules, which means that the LDRA tool suite can successfully document, reference, and ID the specified software code security weaknesses. Meanwhile, TBvision is an automated code test/analysis tool rendering software source-code transparency and providing monitoring of memory errors, quality metrics, test, and security vulnerabilities. Additionally, the LDRA Testbed serves as a software quality-control tool for verification/validation/test, rendering analyses applicable to further dynamic and static analysis.

LDRA • www.mil-embedded.com/p52220 • www.ldra.com

Software helps UAS operators avoid the big jolt

Unmanned Aerial System (UAS) mission operators might have to slog through hundreds of hours of "nothing special" Intelligence, Surveillance, and Reconnaissance (ISR) video. But to avoid the sudden jar-to-life of the "What now?" panic when a noteworthy event *does* occur, AME Unmanned Air Systems' (AME UAS') "SharkFin Basic" UAS mission planning software can help operators plan ahead – and make wise decisions. Specifically, the software provides a triad of mission essentials – payload simulation capabilities, integrated route-planning tools, and unique threat decision aids – all in a single, handy integrated software package.

SharkFin Basic provides 3D situational awareness for UAVs, and is a multi-vehicle, STANAG 4586-compliant Core UAV Control System (CUCS). "Appropriate levels of automation" are provided, to "balance the strengths of computers and humans," the company reports. Though the automation aspect is innate with software, the user-centric interface is scalable and modular, featuring a plug-in architecture compatible with myriad services interfaces. So UAS/UAV mission operators can now breathe a bit easier, knowing that the mission is already planned and that decision tools are in-hand with Sharkfin Basic.

AME Unmanned Air Systems, a ChandlerMay company • www.mil-embedded.com/p52218 • www.ameuas.com

Computers remain useful, even in direct sunlight

Everyone has experienced the frustration: It's a perfectly good computer, tablet, or smartphone, but try to read it in direct sunlight and it's pretty much rendered a useless piece of sophisticated silicon. However, Dontech, Inc. aims to thwart this issue for the warfighter awaiting a SITREP or instruction from Command and Control, thanks to the company's high-brightness Day Vu displays. Combined with Dontech's optical filters, Day Vu displays proffer full readability, even in direct sunlight, with 850 to 1,250 nits as typical on screens diagonally measuring 4.1" to 24".

The "actively enhanced," LED-backlit Day Vu display series is fully customizable and can be configured in multiple ways: 1) with myriad types of touch screens, including resistive touch screens, Surface Acoustic Wave (SAW) touch screens, Projective Capacitative Touch Screens (PCT), Infrared touch screens, and optical imaging touch screens; 2) with antireflective cover glass films offering glare protection via finishes starting at matte 30 gloss and spanning all the way to clear 92 gloss finishes; 3) with transparent heaters, which are "visually transparent substrates with electrically conductive coatings," designed to elongate LCD operating temp ranges from 0 °C to less than -40 °C, for example; and 4) with EMI/RFI shielding, facilitated with 50 to 225 Openings Per Inch (OPI) grid counts, making Day Vu displays suitable for solving EMI/RFI vulnerabilities in accordance with MIL-STD-464 and MIL-STD-461.

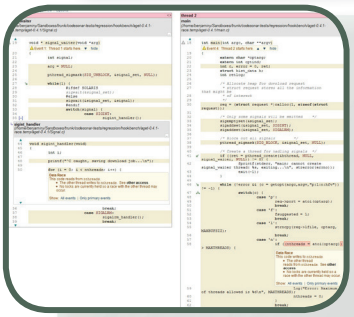
Dontech, Inc. • www.mil-embedded.com/p52219 • www.dontech.com

SSD secure data destruction in less than two seconds

"Mission Impossible" TV show (1966-1973) operatives received their government-centric assignments via a cassette tape recorder embedded with a recorded voice that – after revealing the government top-secret assignment – concluded with the always-true prediction of "This tape will self-destruct in 5 seconds." Though military and government mission-recording technologies have certainly advanced since then, Emphase's MIL-SPEC S5 Series SSD has a similar security capability (but without the automatic smoke): data destruction, fast and secure erasure, and data write protection ensuring data elimination in less than 2 seconds … and so much more.

Providing up to 90 MBps write and 170 MBps read speeds, the MIL-SPEC S5 Series SSD comes in capacities of 16 to 128 GB. (256 and 512 GB iterations are being developed.) Meeting MIL-STD-810F environmentals for thermal shock (-40 °C ~ +85 °C, 10 cycles), drop (Transit Drop Specification), and vibration (20 *g*), the SSD boasts an altitude capacity of 80,000 feet and meets NSA 130-2 specification requirements. With all those credentials, it's not surprising that the SSD is able to call military and defense servers, combat vessels, rugged laptops or tablet PCs, and data and tactical systems "home."

Emphase • www.mil-embedded.com/p52221 • www.emphase.com



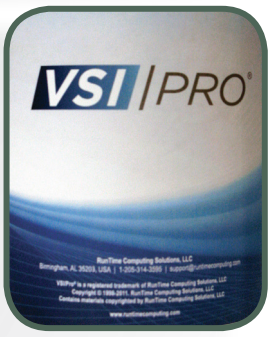
Static analysis advances from one core to … more

Not just a popular engineering trade-show lunchtime topic, multicore processors such as the recently released Intel Core i7 Gen 2 really *are* proving themselves a revolutionary force in speeding up defense and other embedded applications. However, developers know that locating those subtle hiccups in software code can be a real challenge – one that GrammaTech, Inc. aims to thwart with its new multicore program analysis engine. Whereas static analysis tools for single-core software code are relatively polished, multicore static analysis is a tough proposition; that's why DARPA offered GrammaTech a $749,000 contract to produce this new multicore analysis engine.

The engine's mission, true to the static-analysis *modus operandi*, is to search out complex multicore code bugs, particularly those that are intermittent and therefore difficult to spot – without testing. The engine can additionally analyze multithreaded apps on a single processor. Destined for integration on GrammaTech's CodeSonar static-analysis tool, the multicore program-analysis engine – rather than actually running code – renders an abstract model illustrating which of the multicore threads hold which locks, and thereafter analyzes possible interleavings. Compatible with compilers such as Microsoft Visual Studio, CodeWarrior, Green Hills, Intel C/C++, Wind River, ARM RealView, Texas Instruments, and myriad others, this multicore program-analysis engine saves time and finds those bugs missed by overworked developers manually scouring code for errors.

GrammaTech, Inc. • www.mil-embedded.com/p52370 • www.grammatech.com

VSIPL library helps classic DSP stay cutting-edge



DSP apps have been running in the military embedded scene seemingly since the beginning of time. OK, maybe not since the beginning of time, but close … However, even DSP and other signal-processing systems must keep up with the times, and RunTime Computing Solutions' "VSI/Pro 1.20" signal- and math-processing library aims to eliminate porting-to-2nd-gen-Intel-Core woes. Compliant with the Vector, Signal, and Image Processing Library (VSIPL) industry standard for DSP and COTS processor-based image- and signal-processing functionality (www.vsipl.org), VSI/Pro 1.20's optimization for Intel 2nd-Gen Core processors includes vectorized libraries incorporating the new 2nd-gen Core's Advanced Vector Extensions (AVX) instruction set, along with the SSE-based performance enhancements. Note: Though we're focusing on the souped-up Intel Gen 2 version here, RunTime Computing Solutions still offers its PowerPC/AltiVec and x86 versions of VSI/Pro, too.

So what is the "out-of-the-box solution" VSI/Pro's goal in life? To optimize the DSP app's Application Programmer Interface (API) to hasten image- and signal-processing application development and make hand-tuning for particular OS/hardware configurations a thing of the past. The library does that via its provided linear-system and signal-processing functions such as IIR and FIR filters and windowing, 1-D and 2-D correlations and convolutions, and FFTs in 1D, 2D, and 3D style. The option of image-processing functionality is also an alternative.

RunTime Computing Solutions, LLC • www.mil-embedded.com/p52369 • www.runtimecomputing.com

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Crosshairs Editorial

The changing "face" of today's military upgrades is more than skin deep

By Chris A. Ciufo, Editor

We assemble the articles for each issue of *Military Embedded Systems* three to four months in advance, and with so much lead-time, things often change. A lot. Contributors get busy and have to drop out, or new technology announcements are so compelling that we sometimes call up companies and twist their arm to spill their guts. This June issue of *MES* had a lot more churn than normal – which is why you're receiving it later than we'd like. (Sorry about that!) But as we pulled all the articles together at the 11th hour, we spotted a unique pattern: Legacy systems and methodologies are succumbing to the latest technology trends. We're not just referring to the normal march of COTS upgrades; instead, what's revolutionary to me is how "really, really new stuff" is finding its way so darned quickly to the battlefield.

Consider the CWCEC and IDT article about Serial RapidIO and *Intel DSP.* It was only a year ago in March that Curtiss-Wright Controls Embedded Computing privately disclosed to me that their future DSP plans would be oriented around Intel's x86 line. Core 2 Duos were barely shipping on VME and VPX boards, but the Nehalem-based Core i5/i7 had just been announced at the Consumer Electronics Show in Las Vegas. I was shocked that the military's long-standing DSP love affair with the PowerPC could be toppled so quickly. Now, with Sandy Bridge Core i7 SBCs from so many vendors, 64-bit instruction sets and 256-bit Advanced Vector Extensions for floating point are the popular choice for rugged, deployed DSP systems. Wake up, Freescale. Your market is just about gone. But to be fair, we thought we'd balance out the argument by including the article entitled "Power.org celebrates 20 years of advancing Power Architecture technology." Of course, without Freescale's AltiVec road map, it ain't gonna matter much to DoD designers.

Or how about the picture of Dragon Lady on this edition's cover? The U-2 spy plane was publicly supposed to be a NASA platform – at least, that's what the Feds told Russia before one was shot down and Francis Gary Powers became a political prisoner of the Kremlin in May 1960. Check out the size of the B Camera that recorded high-altitude images on the U-2. This was a *huge improvement* over the previous satellite systems that literally took film pictures and ejected a cartridge into space in order to fall to Earth for recovery. (For you young engineers reading this who can't ever remember a world without cell phones, isn't the idea of collecting film from space hilarious?) How quaint the U-2 seems today compared to the loiter capabilities of the Global Hawk and Predator platforms with IR/CITV/EW sensor suites … or of the other "blacker" airframes we don't talk about. America has only been flying UAS platforms for about 10 years (RQ-1 Predator operationally deployed around 2001).

But check this out: Recent reports for soldier-launched UAS ISR platforms under development imply that the video camera in Apple's HD 720p iPhone 4 is so good that contractors are considering just mounting an iPhone 4 in a quasi-disposable drone. That's less than 12 months after the iPhone 4 became publicly available. And Apple is unintentionally making other inroads into defense. Alaska Airlines recently authorized use of the iPad as a digital flight bag to replace the traditional paper navigation and flight books pilots carry. Our article "The iPad factor" shows how today's warfighters – well versed in consumer smartphones, gaming technology, and now tablet computers – are using iPads for embedded, virtual training. It makes perfect sense. Even companies like Black Diamond, noted for their Land Warrior-esque soldier-mounted deployed computers, are using the latest Intel Atom CPUs to bring situational awareness to dismounted soldiers and Special Operations Forces. The Atom processor has only been around for about two years. General Dynamics C4 Systems, on the other hand (literally), is using Android-based PDAs to mount computers on a soldier's wrist. Android has gained traction in the civilian market only in the past two years. As of April, analysts report that Android phones are outselling all other smartphones.

And finally, in what might be the most interesting use of civilian tech rapidly finding its way onto the battlefield, peruse the article "Using DNA to safeguard electrical components and protect against counterfeiting and diversion." Although the company Applied DNA Sciences perfected their "encrypted" plant genome DNA for authentication of clothing (think about those fake Louis Vuitton handbags people crave) and even British currency, the DNA can be added to the ink used to mark semiconductor/IC packages. The DoD is all over this technology as a surefire way of combating the growing problem of counterfeit military ICs entering the supply chain. This biotech start-up has only been around for six years, and now they're poised to do major military service by protecting systems from soldering in gray market or suspiciously procured ICs (like the kind removed from VCRs and PCs by children in third-world countries).

In each of the aforementioned cases – and in the rest of this issue's articles – pay close attention to the shrinking timeframe between cool new civilian tech and the time it takes before it's deployed on the battlefield. The face of platform upgrades has changed. If you blink, you might miss it.

Chris A. Ciufo, Editor
cciufo@opensystemsmedia.com

GE
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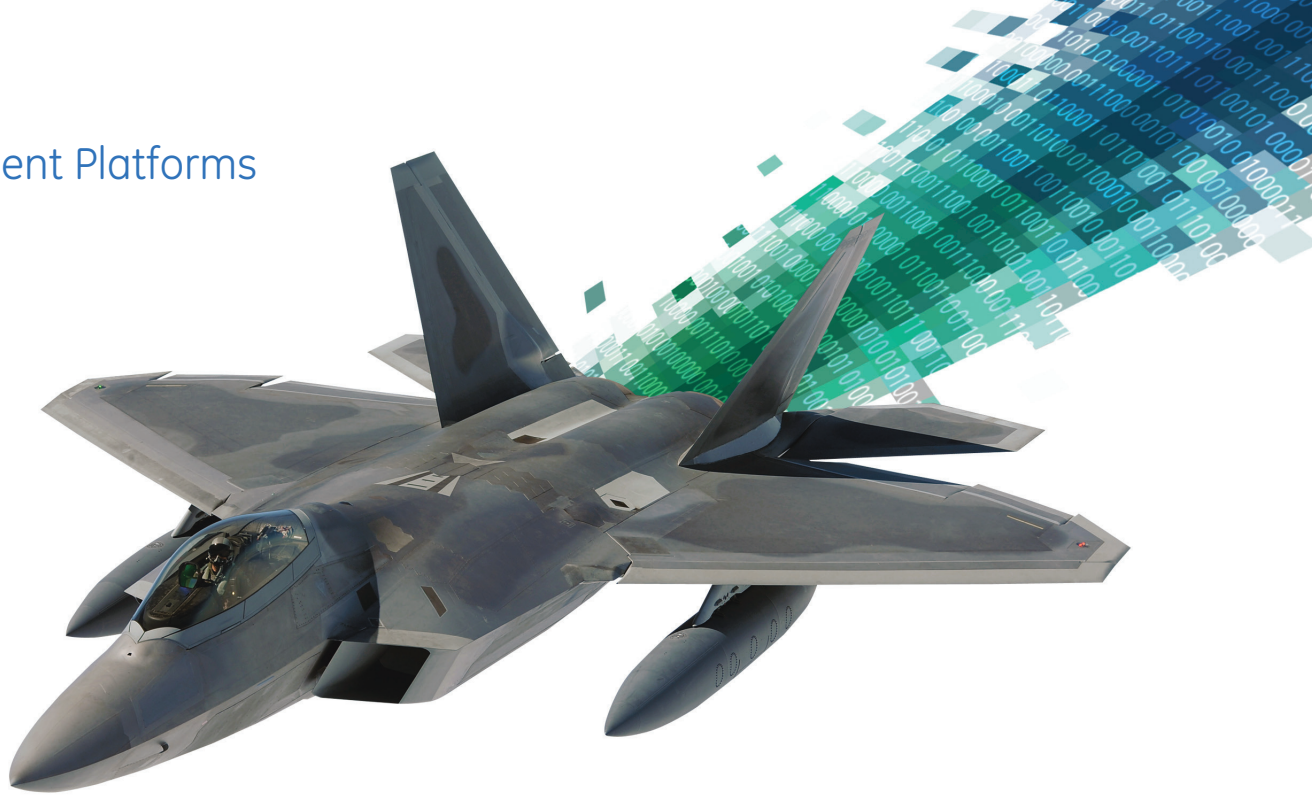

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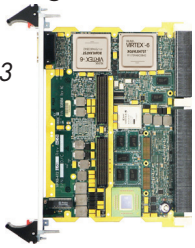

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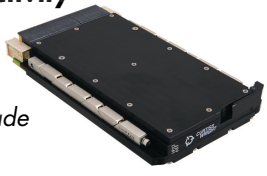

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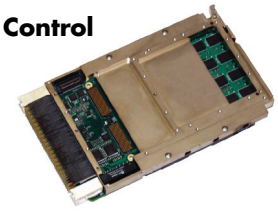

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